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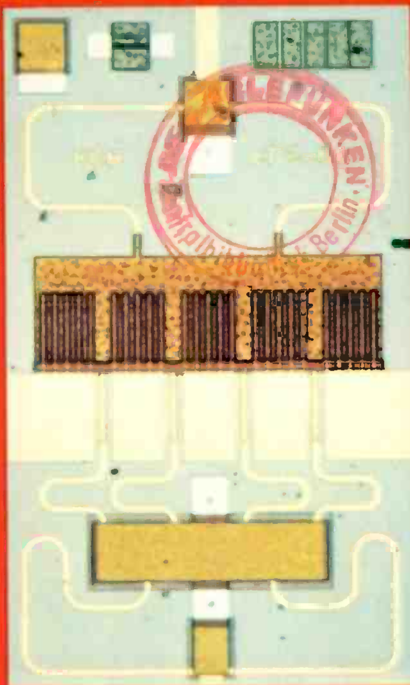

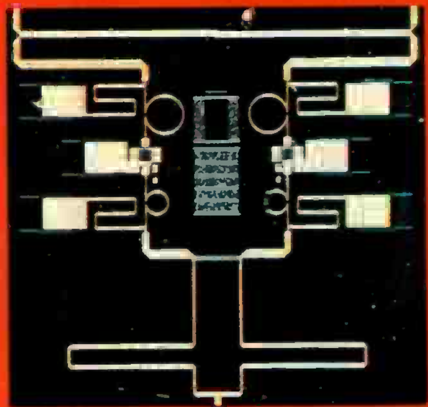

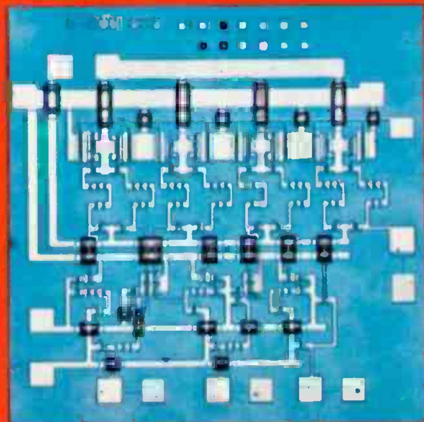

Microwave Technology

December 1981

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Cover

The front cover shows three gallium arsenide monolithic circuits: (left) 8-watt monolithic FET amplifier for S-band operation (1.8 × 3 mm), (upper right) monolithic 0–90° phase shifter for the 4–8 GHz band using dual-gate FETs (4.5 × 4.5 mm), and (lower right) monolithic 3-bit A/D converter operating at gigasample/s rate and containing 58 MESFETs and 55 diodes (1.3 × 1 mm).

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Microwave Technology

Guest Editor: Markus Nowogrodzki

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Foreword to Special Issue on Microwave Technology

Microwave technology is fundamental to a wide range of human activity in modern society. Our air traffic is controlled by microwave radars, our telecommunication networks depend on microwaves to carry their messages, the television shows that we watch are usually distributed by either terrestrial or satellite microwave links, many of us heat our food in microwave ovens, our armed forces use microwaves to detect hostile intruders, to guide weapons, to provide secure communications, and so on. Because of the great importance of microwaves, there is a large, worldwide effort to advance the body of knowledge and techniques that constitute microwave technology. RCA engineers and scientists have made many distinguished contributions to this worldwide effort. Their contributions have ranged from original work on many types of microwave tubes and microwave solid-state devices to large phased-array radars for fleet defense and geostationary satellites that relay communication signals carried at microwave frequencies. Some of the recent contributions to microwave technology by RCA engineers and scientists are described in the papers contained in this special issue of the *RCA Review*.

Nearly half of the papers in this issue reflect a response to the growing need for solid-state components that operate at high microwave or at millimeter-wave frequencies. This need is caused by the congestion of the frequency spectrum at the lower microwave frequencies which forces many users to higher frequencies, and also by the ever-increasing demand by the military for systems that can operate with small antennas and are difficult to detect and jam. There are three papers that report on part of our effort at RCA to extend the operating capability of field-effect transistors to K-band (18–26 GHz) and above. This effort involves optimizing the parameters of conventional GaAs field-effect transistors for high frequency operation (Gordon Taylor et al.), growing new materials with electronic properties that are more favorable to high frequency operation than GaAs (Yegna Narayan et al), and new device structures (Peter Gardner et al). One paper (Arye Rosen et al) explores

the possibility of fabricating monolithic silicon IMPATT circuits for operation at millimeter-wave frequencies. Finally, there are two papers that deal with components and subsystems for solid-state radars operating at 16–16.5 GHz (Henry Johnson and Yehoshua Gazit, and Franco Sechi et al). The 16–16.5 GHz frequency range appears to be particularly useful for small tactical radars, since in this frequency range one can obtain good resolution with moderate size antennas and still have relatively unimpaired operational ability in heavy rain and fog.

The current emphasis in the microwave field on reducing the size and weight of microwave components is illustrated by several papers. One promising approach to miniaturizing microwave components is to replace conventional distributed microstrip circuit components by hybrid lumped element circuit components whenever possible (Jerry Klatskin et al, Adolph Presser, Johnson and Gazit, and F. Sechi et al). Another approach is to monolithically integrate active and passive circuit components on semi-insulating GaAs substrates (Mahesh Kumar et al).

The remaining papers illustrate other important trends in microwave technology. Computer-aided design and optimization are becoming indispensible tools for the microwave engineer (David Rhodes and Jerry Rosen), digital GaAs monolithic circuits that can toggle at microwave rates are becoming available (Chainulu Upadhyayula et al), techniques such as PIN diode switches that were originally developed for microwave applications are being extended to rf frequencies (Phil Basile et al), low-noise GaAs field effect transistor amplifiers when cooled can replace more costly parametric amplifiers (Bob Askew and Herb Wolkstein), and microwave and rf technology are finding important applications in medicine (Fred Sterzer).

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Growth and Characterization of $Ga_xIn_{1-x}As_yP_{1-y}$ and $Ga_{0.47}In_{0.53}As$ for Microwave Device Applications

S. Y. Narayan, J. P. Paczkowski, S. T. Jolly, E. P. Bertin, and R. T. Smith

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Abstract—The vapor phase epitaxial growth and characterization of $Ga_xIn_{1-x}As_yP_{1-y}$ and $Ga_{0.47}In_{0.53}As$ lattice matched to Fe-doped semi-insulating InP substrates is described. The layer composition was measured by electron-probe microanalysis; lattice mismatch by X-ray diffractometry; average carrier concentration and mobility was determined using the Van der Pauw technique; and carrier profiles were investigated using an electrochemical profiler. Quaternary layers with good surface morphology and state-of-the-art electron mobility were grown.

Several hundred n-type $Ga_{0.47}In_{0.53}As$/InP structures were grown and characterized. Unintentionally-doped layers with a carrier concentration of 2.2×10^{15} cm^{-3} and $\mu(300)$ and $\mu(77)$ of 11×10^3 and 27×10^3 $cm^2 V^{-1} s^{-1}$, respectively, were realized. The best $\mu(77)$ was 35×10^3 $cm^2 V^{-1} s^{-1}$ at a doping level of 2.7×10^{15} cm^{-3} and a corresponding $\mu(300)$ of 10.4×10^3 $cm^2 V^{-1} s^{-1}$. Those represent the highest mobility values reported for VPE $Ga_{0.47}In_{0.53}As$ at these doping levels. Se-doped n-layers ranging in thickness from 0.2 to several μm and with carrier density from 1×10^{16} cm^{-3} to 3×10^{18} cm^{-3} were grown. n^+-n structures with sharp n^+-n transitions were grown for device fabrication studies. The doping profile of a 2×1 cm ternary layer grown using a rotating substrate holder was found to be fairly uniform; this n^+-n wafer had an n^+-layer doping of $1.6 \pm 0.1 \times 10^{18}$ cm^{-3}, n^+-layer thickness of 0.31 ± 0.01 μm, n-layer doping of $9.5 \pm 0.5 \times 10^{16}$ cm^{-3}, and n-layer thickness of 0.3 ± 0.03 μm. The mobility profile of submicrometer n-layers was measured using the differential Van der Pauw technique. The high mobility was found to be maintained to the ternary-substrate interface.

1. Introduction

This paper describes the vapor phase epitaxial (VPE) growth and characterization of $Ga_xIn_{1-x}As_yP_{1-y}$ and n-$Ga_{0.47}In_{0.53}As$ lattice matched to semi-insulating Fe-doped InP substrates for high-microwave-frequency field-effect transistor (FET) applications. Theoretical calculations indicate that the $Ga_xIn_{1-x}As_yP_{1-y}$ alloy system, especially for compositions lattice-matched to InP($y = 2.2x$), may have potential for higher low-field mobility and peak drift velocity than GaAs.[1] Experimental investigations show, however, that the electron mobility in this quaternary alloy system exceeds that in GaAs only near the ternary ($Ga_{0.47}In_{0.53}As$) limit.[2,3]

The potential advantages of the $Ga_{0.47}In_{0.53}As$/InP (referred to for simplicity as GaInAs/InP) alloy for high-microwave-frequency FETs are:

(1) High low-field electron mobility. At a doping level of 10^{17} cm^{-3}, the electron mobility in GaInAs can approach 8000 cm^2 V^{-1} s^{-1} compared to about 4500 cm^2 V^{-1} s^{-1} for typical GaAs layers.[1] This high mobility results in lower parasitic resistances and, hence, improved performance, particularly for FETs operating at frequencies of 20 GHz and above.

(2) The peak electron drift velocity in GaInAs is 2.8×10^7 cm/s compared to 2×10^7 cm/s in GaAs.[1] Thus for gate length limits set by technological constraints, GaInAs FETs potential have superior frequency response.

(3) Calculations of the frequency response of submicrometer-gate-length FETs including transient transport effects show that, to a first order, the transit time of electrons under the gate is inversely proportional to $\mu_o \Delta\epsilon_{\Gamma L}$ where μ_o is the low field mobility and $\Delta\epsilon_{\Gamma L}$ is the intervalley energy separation.[4] $\mu_o \Delta\epsilon_{\Gamma L}$ for GaInAs is 4,760 cm^2/s compared to 1520 cm^2/s for GaAs, again indicating its potential for higher frequency operation.[4]

(4) As in the case of GaAs FETs, a semi-insulating substrate (Fe-doped InP) is available. Such a semi-insulating substrate is essential for realizing transistors for high microwave frequencies. Furthermore, since the bandgap of InP (1.34 eV) is greater than that of the ternary (0.72–0.75 eV), the heterojunction interface may assist in confining the electrons to the active layer. This is analogous to the use of GaAlAs buffer layers for GaAs FETs.

The potential disadvantage of GaInAs compared to GaAs for FET applications is that its bandgap is of the order of 0.72–0.75 eV. Typical metal-GaInAs Schottky-barrier heights are about 0.3 eV.[5] To circumvent

problems due to this low Schottky-barrier height, various approaches including p^+n junction gates,[6] heterojunction gates,[7] and MIS gates,[8] are being investigated at many laboratories.

2. VPE Growth System

The VPE growth system used is the hydride synthesis (HCl, Ga, In, AsH_3, PH_3, H_2) process. This system has been used at RCA for the development of light sources and detectors in the 1.0–1.7 μm wavelength range and is described extensively in the literature.[9,10] The VPE system used for opto-electronic devices was modified for our applications. Fig. 1 shows a simplified schematic diagram of the reactor. The key features of this system are:

(1) The Group III metals, In and Ga, are maintained in high-purity quartz boats. Both In and Ga reservoirs are maintained at a nominal temperature of 850°C.
(2) In is transported to the reaction and deposition zones as InCl by reacting it with high-purity HCl gas. Similarly, Ga is transported as GaCl by reacting it with a 10% mixture of high-purity HCl in H_2.
(3) The Group V gases, AsH_3 and PH_3 (10% mixtures in H_2), are premixed and introduced downstream of the In and Ga boats.
(4) Provision is made for n-type doping using dilute H_2Se (nominally 10–20 ppm in H_2) as the doping gas.
(5) The HCl flows are controlled using lengths of stainless-steel capillary tubing in series with accurate pressure regulators. This "constant current source" arrangement is particularly convenient for use with corrosive gases like HCl.

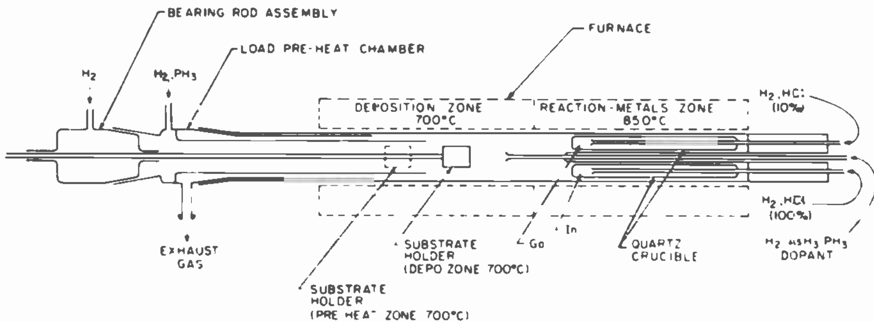

Fig. 1—Schematic of quaternary reactor tube.

(6) The Group V and doping gases are controlled using mass flow controllers.
(7) Arrangements are made to heat (preheat) the InP substrate to growth temperature (nominally 700°C). This is done under PH_3 overpressure to minimize P loss due to dissociation. InP begins to dissociate about 400°C. The preheat zone is downstream of the reactor exhaust; this allows the premixing and stabilization of InCl and GaCl before introducing the substrate into the deposition zone.
(8) The substrate can be rotated at a few revolutions per minute during epitaxial growth to improve uniformity of composition, doping density, and layer thickness across the wafer.

A typical growth run begins by inserting an InP substrate, after suitable cleaning and etching, into the preheat zone and flushing the entire system with pure H_2. The furnace is moved from the standby to the growth position and turned on. An overpressure of PH_3 is maintained over the substrate before the preheat temperature rises to 400°C. Flows of HCl are established over the metals and allowed to stabilize. Once the temperatures have reached steady-state, the AsH_3 and PH_3 flows are set. Composition of the III–V alloy is controlled by the relative flow of the four gaseous species. After stabilization, the substrate is introduced into the deposition zone, thus starting growth. After a specific time, growth is terminated by bypassing the HCl flows over the metals and moving the wafer to the forechamber. The furnace is then moved to the standby position.

The pretreatment of the InP substrates prior to epitaxial growth was found to be critical. We have grown layers on Fe-doped high-resistivity InP substrates provided by Metals Research,* Metal Specialties,† Crystacom,‡ and Sumitomo.§ The etching times for substrates obtained from different vendors were found to be different. Optimum pretreatment procedures were determined for substrates from different vendors by growing ternary test samples. Surface morphology (under Nomarski interference contrast microscopy), lattice mismatch, doping profile, and electron mobility were used as indicators to gauge the efficiency of the pretreatment. The pretreatment includes etching in 5 H_2SO_4:1 H_2O_2:1 H_2O (Caro's acid), 1% Br-methanol etch, 45% KOH soak, and rinsing

* Cambridge Instruments, Inc., Monsey, NY.
† Metal Specialties, Fairfield, CT.
‡ Crystacom, Inc. Mountain View, CA.
§ Sumitomo Electric Industries, Ltd., Hyogo-Ken, Japan.

in deionized H_2O. Highly specular and haze-free epitaxial layers were obtained provided the lattice mismatch was less than 0.3%.

3. Growth of $Ga_xIn_{1-x}As_yP_{1-y}$/InP Alloys

The initial choice of gas flows for the growth of quaternary layers lattice-matched to SI InP substrates was derived from the paper of Hyder, et al.[11] The total carrier gas (H_2) flow was chosen to be 2 *l/m* based on our GaAs epitaxy experience. The first series of experiments consisted of keeping the flow ratio $PH_3/[PH_3 + AsH_3]$ constant and varying HCl(Ga)/[HCl/Ga) + HCl(In)] (also referred to as GaCl/[InCl + GaCl], assuming complete reaction of HCl with In and Ga). The lattice mismatch, composition, bandgap, and electrical properties of the grown layers were then measured. The lattice mismatch was measured by X-ray diffraction techniques; the composition was measured by electron probe microanalysis (EPM); the bandgap was inferred from the measured composition using the curves of Moon et al.;[12] and the electrical properties were determined by the Van der Pauw technique.

Fig. 2 shows the variation of the Ga and As fractions in the III and V sublattices with the normalized HCl(Ga) flow when the Group V gas flows are held constant. Note that the Ga fraction, x, increases linearly with the normalized HCl(Ga) flow while the As fraction, y, remains

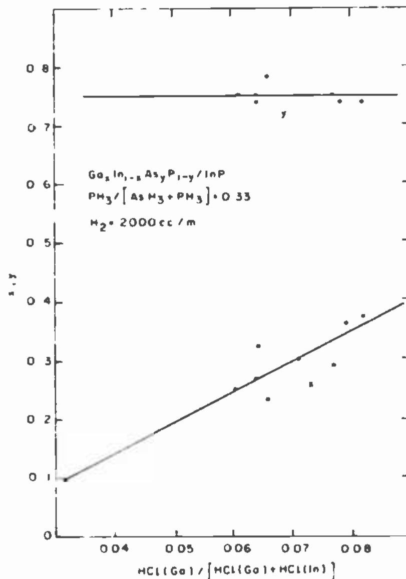

Fig. 2—Variation of x and y with normalized HCl(Ga) flow. Group V flows held constant.

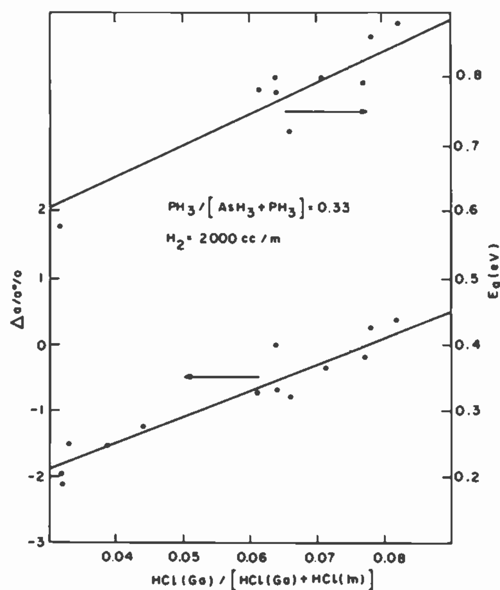

Fig. 3—Variation of E_g and $\Delta a/a$ with normalized HCl(Ga) flow. Group V flows constant.

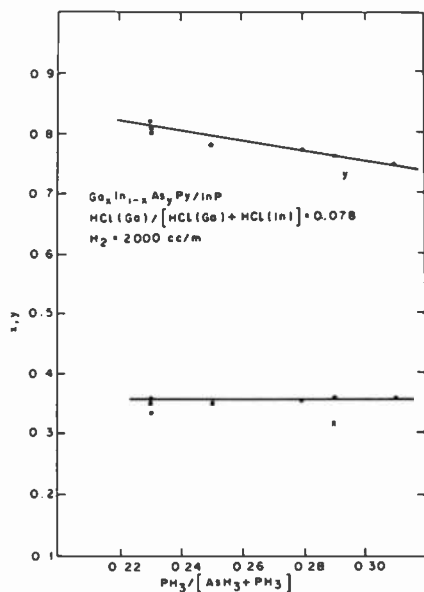

Fig. 4—Variation of x and y with normalized PH_3 flow. Group III flows held constant.

relatively constant as one would expect intuitively. Fig. 3 shows the variation of the lattice mismatch and the quaternary bandgap under the same conditions as in Fig. 2.

The next sequence of calibration experiments were run holding HCl(Ga)/[HCl(Ga) + HCl(In)] constant and varying $PH_3/[PH_3 + AsH_3]$. The carrier gas flow was again maintained at 2 l/m. Fig. 4 shows the variation of x and y with the normalized PH_3 flow. Note that now y can be controlled almost independently of x. Fig. 5 shows the corresponding variations in the bandgap, E_g, and the lattice mismatch $\Delta a/a$. The variation of $\Delta a/a$ is a much weaker function of Group V than Group II gas flows (Fig. 3). The data in Figs. 2–5 allow the preliminary choice of gas flows for a desired quaternary composition. Further iterations are required to fine-tune the bandgap and attain zero lattice mismatch. Table 1 lists the properties of some of the quaternary layers grown. The III–V ratio in the gas phase was maintained at 0.5. This value resulted in the best compromise between surface morphology and electron mobility.

Fig. 6 shows the experimentally measured quaternary mobility at 300 K as a function of composition. Experimental data available in the literature are also shown.[2,3] Note that our mobility values are comparable. The mobilities are also a function of the carrier concentration. Fig. 6 is

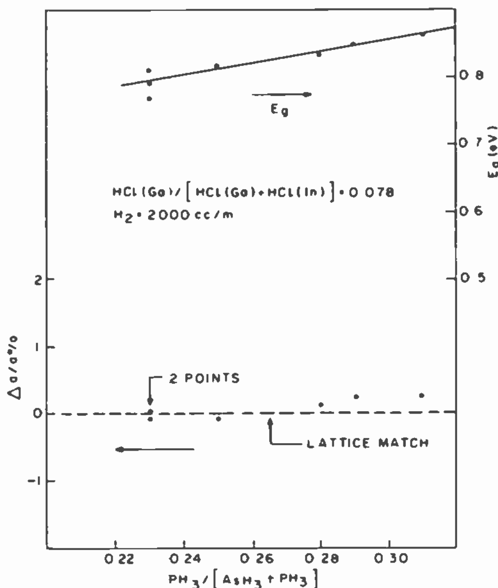

Fig. 5—Variation of E_g and $\Delta a/a$ with normalized PH_3 flow. Group III flows held constant.

Table 1—Properties of $Ga_xIn_{1-x}As_yP_{1-y}$/InP Layers

Wafer No.	Composition* x	Composition* y	Lattice Mismatch $\Delta a/a$ %	$(N_D - N_A)$ cm^{-3} 300 K	$\mu(300)$ $cm^2 V^{-1} s^{-1}$	$(N_D - N_A)$ cm^{-3} 77 K	$\mu(77)$ $cm^2 V^{-1} s^{-1}$	E_g eV
Q27	0.32	0.75	~0					0.8
Q36	0.1	0.82	−2.1	4.4 E16	6.75×10^3	4 E16	11.9×10^3	0.6
Q37	0.25	0.75	−0.73	3 E16	5.83×10^3	3 E16	9.2×10^3	0.78
Q42	0.23	0.78	−0.77	3.4 E16	4.48×10^3	3.4 E16	7.62×10^3	0.72
Q43	0.30	0.75	−0.32	2.8 E16	4.54×10^3	2.3 E16	6.33×10^3	0.80
Q44	0.29	0.75	−0.18	2.3 E16	3.97×10^3			0.79
Q46	0.37	0.74	+0.4	1.5 E16	3.91×10^3			0.88
Q47	0.36	0.74	+0.3	1 E16	4.79×10^3			0.86
Q49	0.36	0.76	+0.23	1.6 E16	4.37×10^3	1.2 E16	8.2×10^3	0.85
Q53	0.36	0.81	~0	1.45 E16	3.96×10^3	1.0 E16	6.52×10^3	0.81
Q57	0.43	0.94	~0	1.4 E16	5.76×10^3	1.1 E16	11.5×10^3	0.75

* Composition measured by electron-probe microanalysis is accurate to ±2% (relative).

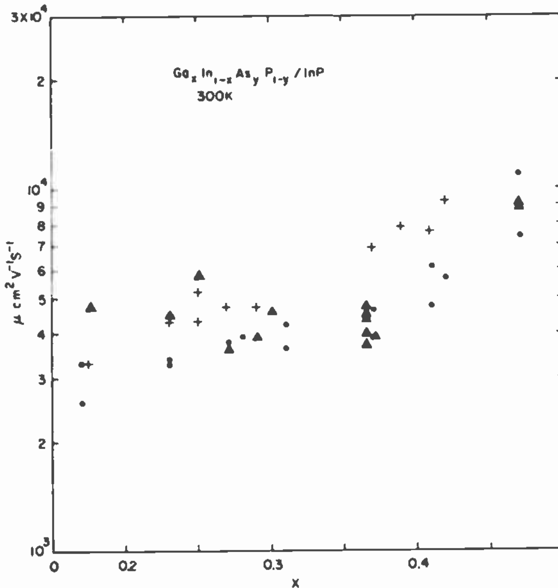

Fig. 6—Electron mobility as function of composition for $Ga_xIn_{1-x}As_yP_{1-y}$/InP ($y = 2.2\ x$). ▲ our data; + Greene, et al.[2]; ● Leheny, et al.[3] Note mobility is also a function of carrier concentration. This figure shows the general trend.

intended merely as a survey to indicate general trends and must be interpreted accordingly. It is clear that the mobility increases as we approach the ternary boundary.

4. Growth of $Ga_{0.47}In_{0.53}As$/InP

Several hundred n-GaInAs/InP layers have been grown for material and device studies. Fig. 7 shows the room temperature electron mobility, $\mu(300)$, of a number of samples plotted as a function of the free electron density. The line shows the typical electron mobility in GaAs for a compensation factor, $(N_D + N_A)/(N_D - N_A)$, equal to 2.[13] It is clear that this ternary layer has higher electron mobility than GaAs of equivalent doping. The highest $\mu(300)$ measured was 11×10^3 cm^2 V^{-1} s^{-1} at a doping level of 2.2×10^{15} cm^{-3}. The corresponding $\mu(77)$ was 27×10^3 cm^2 V^{-1} s^{-1}. The best 77 K mobility was 35×10^3 cm^2 V^{-1} s^{-1} at a carrier level of 2.7×10^{15} cm^{-3} with a corresponding $\mu(300)$ of 10.4×10^3 cm^2 V^{-1} s^{-1}. These represent the highest values reported for VPE GaInAs/InP at this doping level. Fig. 8 shows some of the lattice mismatch ($\Delta a/a$) values measured. The surface morphology of the ternary layers was excellent when $\Delta a/a$ is less than 0.3%.

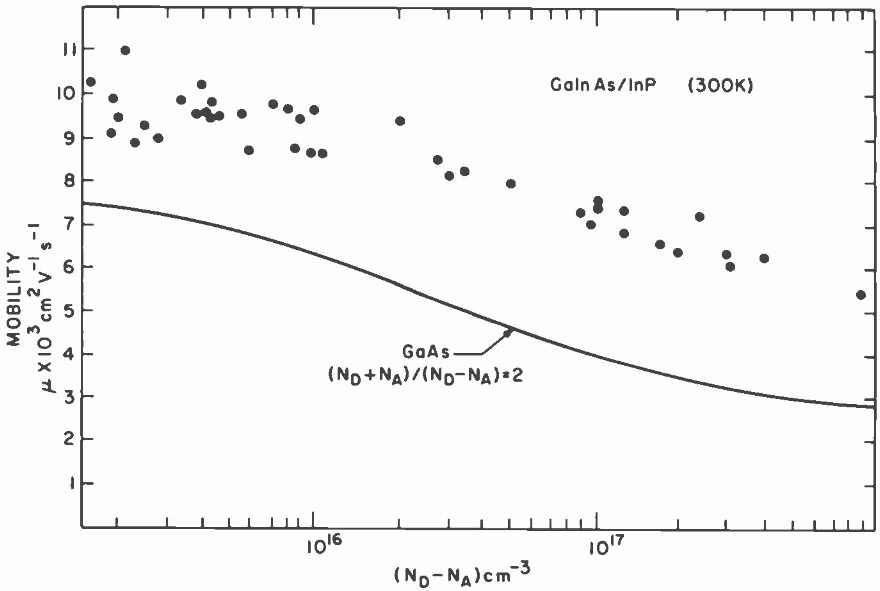

Fig. 7—Electron mobility of $Ga_{0.47}In_{0.53}As$ at 300 K as function of carrier concentration.

Fig. 9 shows $\mu(300)$ and $\mu(77)$ of a number of ternary layers as a function of free electron concentration. Calculated curves based on a simple theory are also shown.[14] This heuristic calculation uses the relaxation time approximation and includes the effects of polar optical, random alloy, and impurity scattering. The electron mobility is obtained by combining the component values using Mattheissen's rule ($\mu^{-1} = \Sigma_i \mu_i^{-1}$). The compensation factor, $(N_D + N_A)/(N_D - N_A)$, appears to be between 2 and 5 to within the limitations of the calculation. A recent publication indicates that use of Matthiesen's rule overestimates $\mu(300)$

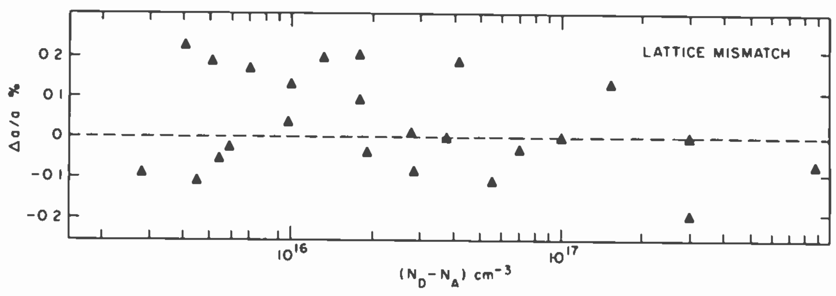

Fig. 8—Lattice mismatch of $Ga_{0.47}In_{0.53}As/InP$ layers. ($N_D - N_A$ is used to separate points; there is no functional relationship.)

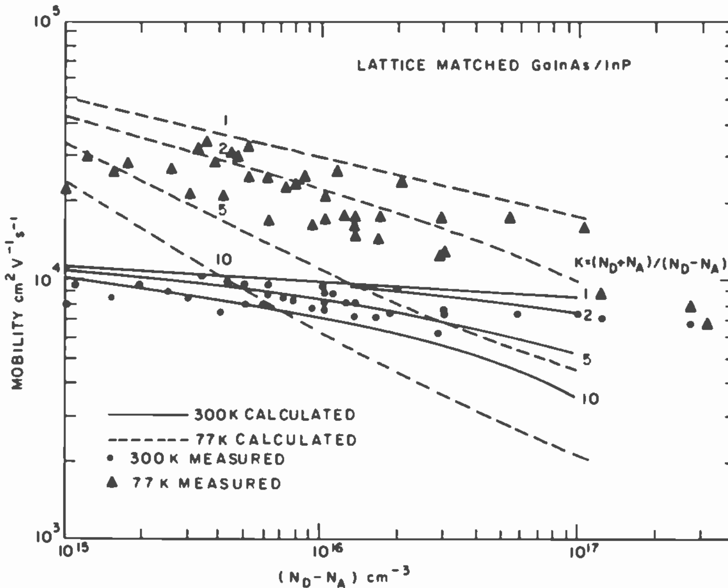

Fig. 9—Calculated and measured $\mu(300)$ and $\mu(77)$ for $Ga_{0.47}In_{0.53}As/InP$.

by 10–15%.[15] Furthermore, Matthiesen's rule results in a temperature variation of mobility different from that experimentally observed. This implies that the compensation factor of our material is closer to 2 than 5.

The carrier density profiles were measured using an electrochemical profiler* developed by the British Post Office Research Center.[16] This instrument employs a novel technique developed by Faktor and Ambridge.[16] The semiconductor sample is loaded in an electrochemical cell wherein a small dc voltage is applied to produce a reverse bias to the semiconductor-electrolyte Schottky-barrier system causing continuous electrolytic etching (under illumination for n-type material). The bias is adjusted so that the Schottky diode does not break down, and the capacitance and hence, doping density is measured using suitable analog circuitry. The capacitance and voltage are monitored *in situ* as the etch progresses and a continuous doping profile is produced. The limitation of low Schottky-breakdown voltage is thus overcome. A current integrator determines the thickness etched according to *Faraday's law of electrolysis*.

The depth determined by the profiler was compared with the depth of the etched hole measured by a mechanical stylus gauge and found to

* Polaron Semiconductor Profile Plotter, Polaron Equipment Ltd., England.

be very accurate. The carrier concentration measured is in reasonable agreement with the average value measured by the Van der Pauw technique. For example, on wafer Q473, a carrier concentration of 2.9×10^{16} cm^{-3} and layer thickness of 0.45 μm was measured. The average carrier concentration measured by the Van der Pauw technique was 2.6×10^{16} cm^{-3}.

The doping profile of a number of samples was measured. Fig. 10 shows a typical profile of a Se-doped n-layer. Note the uniform carrier profile. Fig. 11 shows three traces measured along the diagonal of a 2×1 cm n^+-n wafer grown using the rotating wafer holder. Note the sharp n^+-n interface. The doping density of the n-layer is $9.5 \pm 0.5 \times 10^{16}$ cm^{-3} and the epilayer thickness is 0.6 ± 0.025 μm across this wafer, a reasonable uniformity.

The study of doping profiles across a wafer is important from both material characterization and device development viewpoints. Van der Pauw measurements on a layer with inhomogeneous doping can give either erroneously low or anomalously high values for electron mobility.[17] Fig. 12 is a doping profile of a layer with a doping peak close to the interface and obviously unsuitable for device fabrication studies.

Fig. 13 shows two examples of the doping and mobility profiles for ternary layers measured by the differential Van der Pauw method.[18]

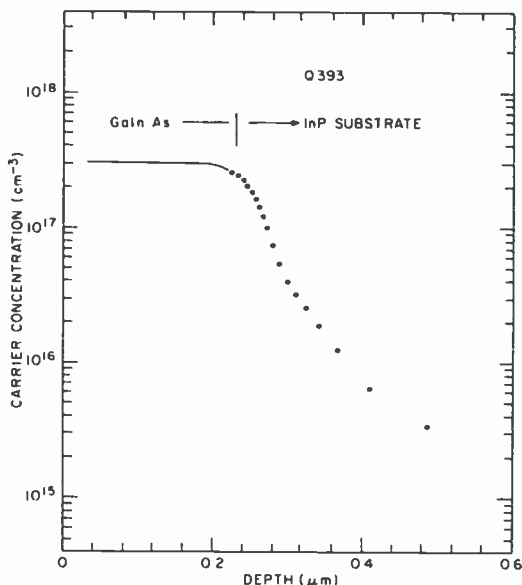

Fig. 10—Carrier profile of a n-$Ga_{0.47}In_{0.53}As$/InP wafer measured using the Polaron electrochemical profiler.

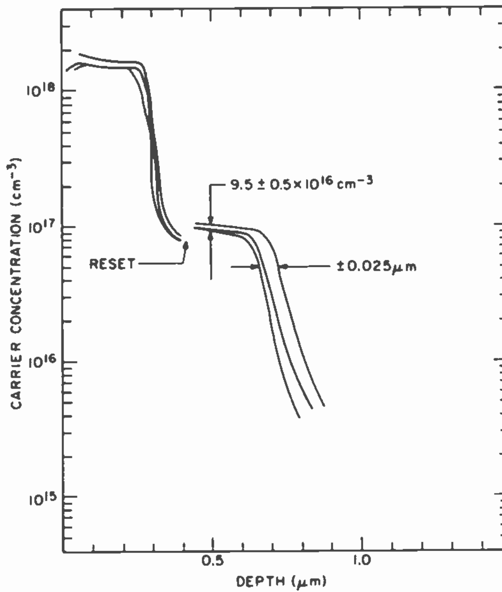

Fig. 11—Carrier profiles measured across the long diagonal of a 2 × 1 cm $Ga_{0.47}In_{0.53}As/InP$ wafer. The machine was reset after profiling n^+-layer resulting in an offset at n^+-n interface.

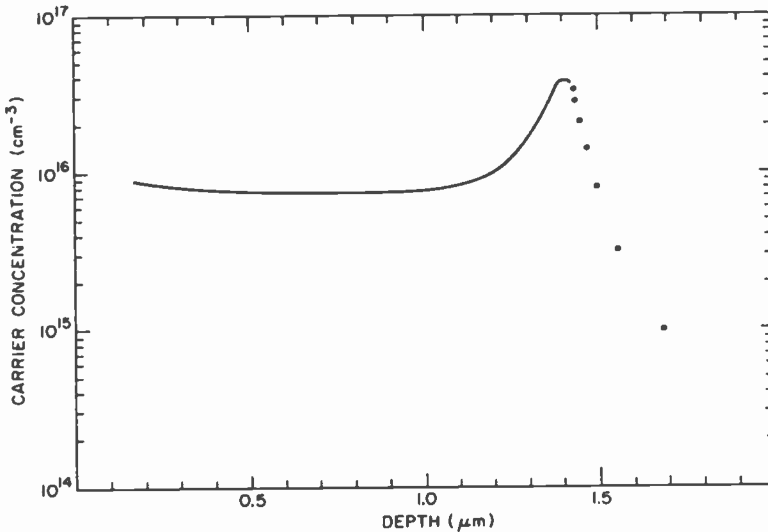

Fig. 12—Carrier profile of $Ga_{0.47}In_{0.53}As/InP$ wafer with doping peak near substrate interface.

Note that the electron mobility is fairly constant to the substrate interface.

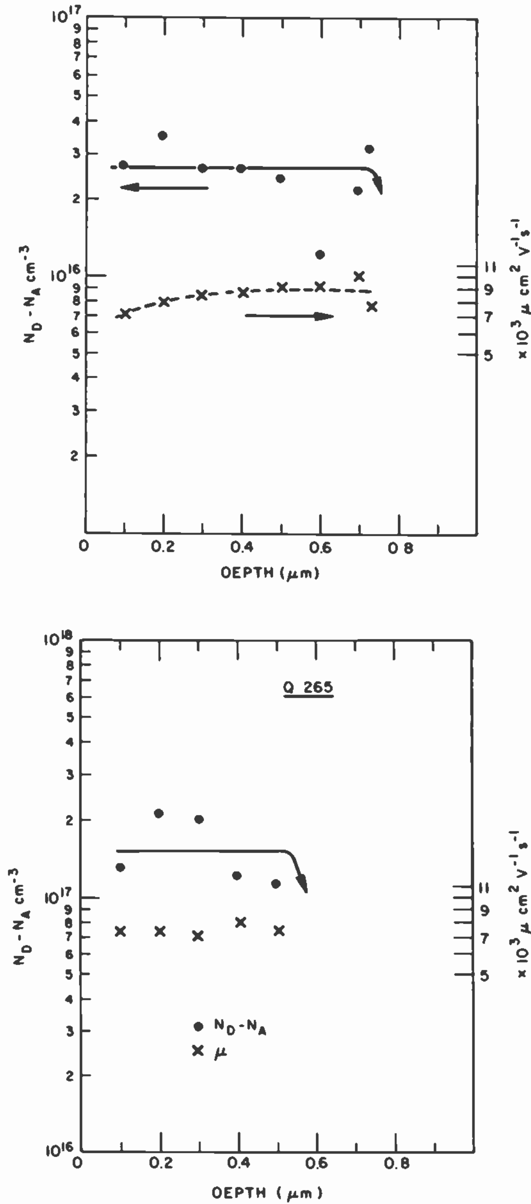

Fig. 13—Carrier density and mobility profiles measured by differential Van der Pauw technique. Note mobility is maintained up to the ternary-substrate interface.

Table 2 shows the variation of the composition and lattice mismatch over typical ternary wafers. The composition and mismatch are fairly

Table 2—Uniformity of 2 × 1 cm Ternary Layers as Measured by X-Ray Diffractometry and by Electron-Probe Microanalysis (Electron-Probe Microanalysis Is Accurate to ±2% Relative)

Wafer No.	X-Ray Diffractometry $\Delta a/a$(%)	Electron-Probe Microanalysis Ga	In	As	P	General Comments
Q414						
Leading Edge	0.00	0.44	0.56	1	0	Stationary substrate holder
Center	0.00	0.43	0.57	0.96	0.04	
Trailing Edge	0.00	0.43	0.57	0.97	0.03	
Q418						
Leading Edge	—	0.45	0.55	1	0	Stationary substrate holder
Center	—	0.44	0.56	1	0	
Trailing Edge	—	0.43	0.57	0.98	0.02	
Q444						
Section A	0.00	0.43	0.57	1	0	Rotating substrate holder
Section B	0.05[a]	0.43	0.57	1	0	
Section C	0.07[a]	0.45	0.55	1	0	
Q445						
Section A	0.27/0.55[b]	0.46	0.54	1	0	1. Rotating substrate holder
Section B	0.35/0.58[b]	0.47	0.53	1	0	2. Doping profile had very poor and broad layer-substrate interface
Section C	−0.13/0.15/0.46[c]	0.46	0.54	1	0	
Q447						
Section A	0.07	0.44	0.56	1	0	Rotating substrate holder
Section B	0.00	0.43	0.57	1	0	
Section C	−0.06	0.42	0.58	1	0	
Q480						
Center	0.05	0.44	0.56	1	—	Rotating substrate holder
Q481						
Center	0.05	0.44	0.56	1	—	Rotating substrate holder
Q493						
Section A	0.05	0.39	0.61	1	—	1. Rotating substrate holder
Section B	0.05	0.41	0.59	1	—	2. Porous quartz baffle
Section C	0.04	0.41	0.59	1	—	3. Better doping uniformity
Q495						
Section A	0.05	0.44	0.56	1	—	Same as Q493
Section B	0.00	0.43	0.57	1	—	
Section C	0.00	0.44	0.56	1	—	

[a] Assymetric broadening indicates slight gradient towards positive mismatch.
[b] Two descrete phases.
[c] May be three broadened but discrete phases.

constant across the whole wafer. These results show that GaInAs layers with excellent mobility, flat doping and mobility profiles, and good surface morphology can be grown lattice-matched to InP substrates.

5. Conclusions

A hydride vapor synthesis reactor was developed for the growth of n-type $Ga_xIn_{1-x}As_yP_{1-y}$ alloys for microwave device applications. Ga_xIn_{1-x}-As_yP_{1-y} and $Ga_{0.47}In_{0.53}As$ layers lattice-matched to Fe-doped, semi-insulating InP substrates were grown and characterized. The layer composition was measured by electron-probe microanalysis; lattice mismatch determined by X-ray diffractometry; average carrier concentration and electron mobility were measured by the Van der Pauw technique; and carrier profiles were studied using an electrochemical profiler. Quaternary layers with good surface morphology and state-of-the-art electron mobility were grown.

Several hundred n-type $Ga_{0.47}In_{0.53}As$ layers lattice-matched to Fe-doped InP substrates were grown and characterized. Layers grown without intentional doping were n-type with background carrier densities as low as 1×10^{15} cm^{-3}. Layers with 300 K electron mobility $[\mu(300)]$ as high as 11×10^3 cm^2 V^{-1} s^{-1} at carrier levels of 2.2×10^{15} cm^{-3} and 77 K electron mobility $[\mu(77)]$ of 27×10^3 cm^2 V^{-1} s^{-1} were grown. The highest $\mu(77)$ measured was 35×10^3 cm^2 V^{-1} s^{-1} at a carrier level of 2.7 $\times 10^{15}$ cm^{-3} with a corresponding $\mu(300)$ of 10.4×10^3 cm^2 V^{-1} s^{-1}.

Se-doped n-layers were grown that ranged in thickness from 0.2 to several micrometers with carrier densities from 1×10^{16} to 3×10^{18} cm^{-3}. n^+-n structures with sharp n^+-n transitions were grown for device fabrication studies.

The doping profile of a 2×1 cm ternary layer grown using a rotating substrate holder was found to be fairly uniform; this n^+-n wafer had an n^+-layer doping of $1.6 \pm 0.1 \times 10^{18}$ cm^{-3}, n^+-layer thickness of 0.31 ± 0.01 μm, n-layer doping of $9.5 \pm 0.5 \times 10^{16}$ cm^{-3}, and n-layer thickness of 0.3 ± 0.03 μm. The mobility profile of submicrometer n-layers was measured using the differential Van der Pauw technique. The high mobility was found to be maintained to the ternary-substrate interface.

Acknowledgments

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GaAs Power Field-Effect Transistors for K-Band Operation

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Abstract—This paper reports on developments in device processing leading to flip-chip mounted GaAs power FETs capable of operating at X- and K-band frequencies. The principal development concerns a technique for producing FETs with submicrometer gate lengths by making use of the undercut associated with chemical etching. GaAs FETs fabricated using this process have operated at frequencies as high as 26 GHz. At 18 GHz, an output power of 360 mW at 4.4 dB with 26.8% power added efficiency was obtained. At 26 GHz, 55 mW at 3-dB gain with 5% power-added efficiency was demonstrated.

1. Introduction

Much progress has been made in the last few years in extending the frequency of operation and power handling capabilities of GaAs power field-effect transistors. This progress has been the result of improvements in device fabrication techniques in conjunction with advances in the quality of GaAs substrates and GaAs active layers produced by either epitaxy or ion-implantation. This paper will concentrate only on some recent developments in device processing technology that has resulted in GaAs power FETs capable of operating at K-band frequencies. The principal development concerns a technique for producing FETs with submicrometer gate lengths by making use of the undercut associated with chemical etching. GaAs FETs fabricated using this technique have operated at frequencies as high as 26 GHz. These devices are designed

to be flip-chip mounted by a process developed previously at RCA and documented in earlier reports.[1] This flip-chip GaAs FET design leads to both low thermal impedance and low parasitic source inductance. Since the fundamental design, advantages of flip-chip mounting, and thermal impedance considerations have been described in Ref. [1], they will not be dealt with here.

2. Design Considerations

Although considerable work is taking place in modeling GaAs FETs, the power gain, output power, and power-added efficiency of these devices cannot yet be adequately predicted from the device structure and the measurable characteristics of the GaAs starting material. However, some insight about how device structures can effect performance can be obtained from existing small-signal device models. Fig. 1 is a simplified equivalent circuit model of an FET. The analytical expressions for the model elements derived by Pucel, et al.[2] are as follows:

$$R_m = \frac{p_m Z}{3 L_g t_g} \qquad [1]$$

$$C_{sg} = 2k\epsilon_0 Z \left\{ \frac{L_g}{a} \left(\frac{1}{1 - I_d/I_s} \right) + 1.56 \right\} \qquad [2]$$

$$R_s = R_c + R_{sc} = \frac{(p_c/nq\mu a)^{1/2}}{Z} + \frac{L_{sg}}{nq\mu a Z} \qquad [3]$$

$$g_m = 4k\epsilon_0 v_s (Z/a) \left\{ \frac{1}{1 - I_d/I_s} \right\} \qquad [4]$$

$$g_{m_{eff}} = \frac{g_m}{1 + g_m R_s} \qquad [5]$$

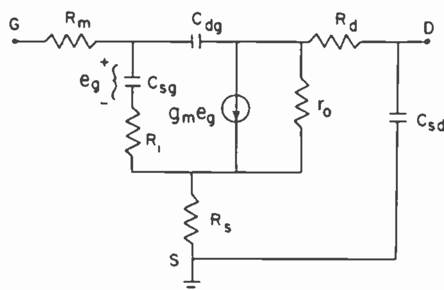


Fig. 1—Equivalent circuit small-signal model of GaAs FET.

where

p_m = gate metal resistivity
Z = width of device channel (long dimension of gate)
L_g = gate length (short dimension of gate)
t_g = thickness of gate metallization
$K\epsilon_o$ = dielectric constant of GaAs
a = thickness of active device channel under gate
p_c = specific contact resistance of the ohmic contacts
n = channel doping density
q = electron charge
μ = electron mobility in channel
L_{sg} = spacing between the source contact and the gate
v_s = saturation velocity of electrons in GaAs
I_d = drain current
I_s = maximum current of the fully-undepleted channel

To achieve the best high frequency performance, it is obvious that the parasitic resistances and capacitances, such as R_m, C_{sg}, R_s, and R_d must be made as small as possible and that the transconductance, g_m, and drain output resistance, r_o, must be as large as possible. To minimize the source-to-gate capacitance, C_{sg}, it is necessary to keep the gate length L_g small to reduce the L_g/a term in the expression for C_{sg}. The gate resistance, R_m, is directly proportional to the metal resistivity and inversely proportional to the gate length, L_g, and metal thickness, t_g. Therefore, to minimize the gate metal resistance without increasing the source-to-gate capacitance, C_{sg}, the gate metallization should be as thick as possible. The constant term within the bracket in the expression for C_{sg} (Eq. [2]) represents the contribution due to fringing capacitance so that there is a point where reducing the gate-length-to-channel-thickness ratio, L_g/a, further would not appreciably reduce C_{sg}. Experimental evidence indicates that the L_g/a ratio cannot be made arbitrarily small without causing a decrease in g_m and r_o. However, smaller gate lengths have demonstrated an advantage at least down to the 0.5-μm range.

To minimize C_{sg} while maintaining a low value of gate resistance, we employ a gate with a "T"-shaped cross-section. The effective gate length is made small by lateral etching of the bottom metal layer of the gate to reduce the length of gate in contact with the GaAs. The top section of the gate is left longer to keep the gate resistance low. This simultaneously satisfies the conflicting requirements that L_g be small to reduce C_{sg} and large to reduce R_m.

The source-to-gate resistance R_s consists of two components—the contact resistance R_c between the ohmic metal and the GaAs and the channel resistance R_{sc} between the edge of the source and the gate. It

is very important to reduce R_s, not only to decrease the power lost in this resistance but because it feeds back a voltage to reduce the effective transconductance of the device as given in Eq. [5]. R_{sc} can be reduced by minimizing the spacing between the source and gate L_{sg}, but a gap on the order of 1 to 1.5 μm is usually required to allow for misalignment tolerance. A gate recess structure, which maintains a thicker channel up to the edge of the gate, can also be used to reduce R_{sc}. The contact resistance R_c is a function of the metallization used but is roughly proportional to the reciprocal of the electron concentration, n^{-1}. R_s can therefore also be reduced by increasing the doping density of the channel. However, the doping density cannot be made arbitrarily large without degrading channel mobility and reverse gate-breakdown voltage. Instead of increasing the doping density of the entire channel, a practical solution is to introduce highly-doped material locally in the source and drain areas. For epitaxially-grown device layers, this involves growing the channel layer on the semi-insulating substrate and then capping it with a highly-doped n^+-layer. The n^+-layer is removed from the region of the gate in the early stages of device processing prior to depositing the Schottky barrier gate.

3. Device Fabrication

Fig. 2 is a cross-sectional view of the FET structure employing a highly-doped ($1 \times 10^{18} cm^{-3}$) n^+ layer under the ohmic source and drain contacts. A 3-μm wide channel recess is used to maintain a separation between the n^+-layer and the gate metal. A 1-μm-wide gate recess is used

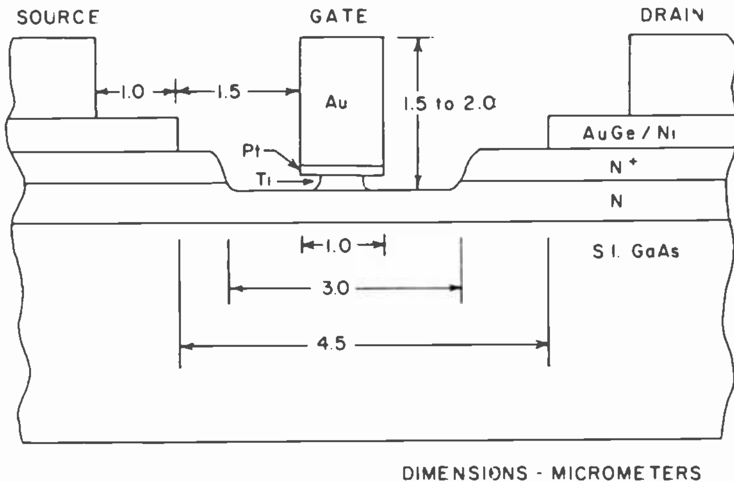


Fig. 2—Cross section schematic of one channel of FET structure.

to reduce the channel current to the desired value and to improve the source-to-drain burnout and gate-to-drain breakdown voltages.[3,4] For active layers produced by ion-implantation, the n^+-layer is not used because of limitations in the thickness of the implanted layers at moderate implant energies (~250 keV).

Device processing starts by etching away the n^+ and n layers outside the active device regions to form mesa structures. Ohmic contacts are produced by simple photoresist lift-off of AuGe/Ni/Au and subsequent sintering at 450°C for 60 seconds in a forming-gas ambient. The channel recess and gate recess are then etched to adjust the device saturation currents to the desired value.

As described earlier, the conflicting requirement of small gate length for low source–gate capacitance and wide gate length for low gate-metal resistance can be satisfied by producing a "T"-shaped gate cross-section. A process was developed to produce this type of gate by a lift-off of Ti/Pt/Au gate metallization followed by simple chemical etching of the Ti layer. The initial gate length is nominally 1 μm, which is close to the smallest dimension practical for standard UV contact lithography. A chemical echant for Ti is used to undercut the Pt/Au layers of the gate to reduce the gate length to the submicrometer range without appreciably increasing the gate-metal resistance. Additional reduction in the gate-metal resistance was obtained by increasing the gate-metal thickness. A dramatic increase in the thickness obtainable by the lift-off technique has been achieved by using a double photoresist layer process.[5]

The processing sequence for gate lift-off is illustrated in Fig. 3. At this step of device fabrication, the ohmic contacts, mesa structure and gate recess have been completed. The gate process starts with deposition of a layer of Ti over the entire substrate. The thickness of this layer is important and will influence the lateral etching rate during the chemical etching step. Typically, the Ti layer is 1000 Å thick. After metallization of the wafer, a layer of photoresist is applied and prebaked. This layer, approximately 1.5 μm thick, serves as a lift-off assist layer and also aids in smoothing out the surface topology. As illustrated in Fig. 3a, a 3-μm-wide gate mask is then used to expose this photoresist layer; however, it is not developed until later. A thin, transparent layer of Ti is evaporated next to protect this layer while the top photoresist layer is spun on. A nominal 1-μm gate opening is patterned in the top photoresist layer as illustrated in Fig. 3b. After developing the top photoresist layer, the transparent Ti layer is then chemically etched away to expose the bottom photoresist layer. The bottom layer of photoresist is then developed to produce an undercut photoresist profile as shown in Fig. 3c.

The Ti/Pt/Au gate metallization is evaporated using the opening in

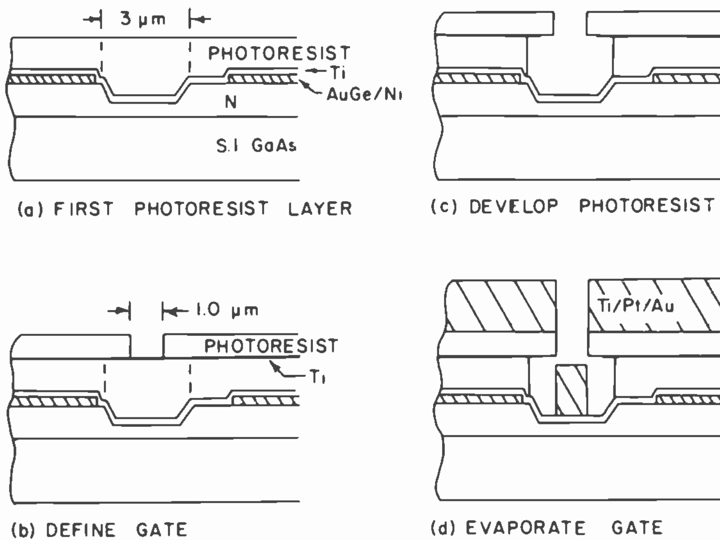


Fig. 3—Process sequence for lift-off gate fabrication.

the top photoresist layer to define the gate region. After the gate metal is deposited, lift-off of undesired metal is achieved by dissolving the photoresist in organic solvents. This undercut photoresist profile is ideal for the lift-off process since it maintains a gap between the gate metal and the metal deposited on top of the photoresist. This eliminates the ragged edges usually produced by the lift-off process.

Thick gate metallization is desirable to reduce the gate-metal resistance and to improve the step coverage of the gate metallization where it crosses the edge of the mesa. For these reasons a study was made to determine the limits of gate metallization thickness that can be achieved with good yield. Intuitively, one would expect that the use of a double photoresist layer would allow the lift-off of metallization up to a thickness equal to that of the bottom photoresist layer. It was found, however, that this technique can be used to produce gate metallization much thicker than the bottom photoresist layer. Examination of an SEM of a sample cleaved through the gate region after gate metal evaporation but before lift-off revealed how this occurs. Deposition of metal on the sidewalls of the gate opening of the top photoresist layer causes the opening to narrow during the evaporation. As a result, the gate also narrows as it grows higher, thereby maintaining a gap between the gate and the metal deposited on top of the photoresist. This can be seen in Fig. 4 which shows a 1.8-μm-thick gate prior to lift-off. Although the photoresist was distorted slightly by cleaving the sample, the narrowing of the gate at the top and of the gap between the gate and the overlying metal layer are clearly shown.

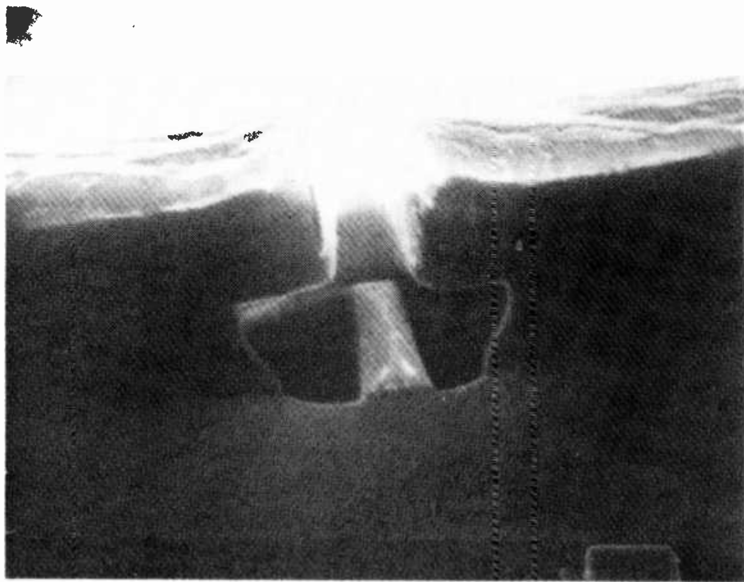


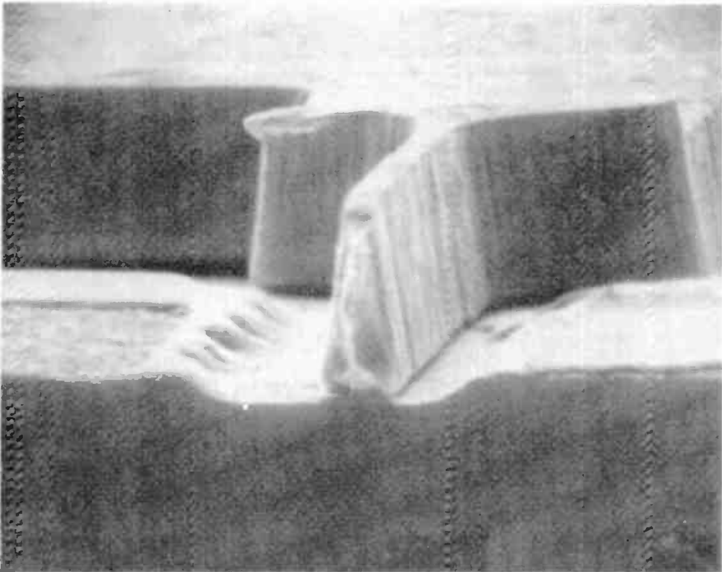
Fig. 4—Scanning electron micrograph of a cleaved cross-section of wafer C866 after gate metal evaporation but before lift-off. Magnification 10,000X; gate metal thickness = 1.8 μm.

The thickest gate metallization produced to date was 3.0 μm on wafer B760. Cross-sectional views of a gate on this wafer are shown in Fig. 5. The sample was prepared for SEM examination by cleaving the wafer across the device channel. Fig. 5a shows a view looking from the device channel toward the gate pad. A notch can be seen where the gate crosses the 0.6-μm mesa step. Such a thick gate has excellent step coverage at the mesa edge. As shown in Fig. 5b, the gate narrows to about 0.5 μm at the top from the 1.25-μm gate length at the base. This is caused by gate metal deposition on the sidewalls of the gate opening in the top photoresist layer. That the top of the 3-μm thick gate is very smooth indicates that there is still a clear separation between the gate and the metal deposited on top of the photoresist layer.

After lift-off patterning of the gates, the gate length is in the range of 1.0–1.25 μm. A chemical etchant[6] for Ti is then used to reduce the physical gate length to submicrometer dimensions by etching the bottom Ti layer, as illustrated in Fig. 6. Good control of the gate length was achieved by this simple technique. Figs. 7a and b show cross sections of the gate after Ti etching for a total of 1.75 minutes and 3.5 minutes, respectively. The gate length achieved by etching for 3.5 min is in the range of 0.5–0.6 μm.

Whenever lateral etching is used to produce such narrow lines, the

(a)
10,000X



(b)
20,000X

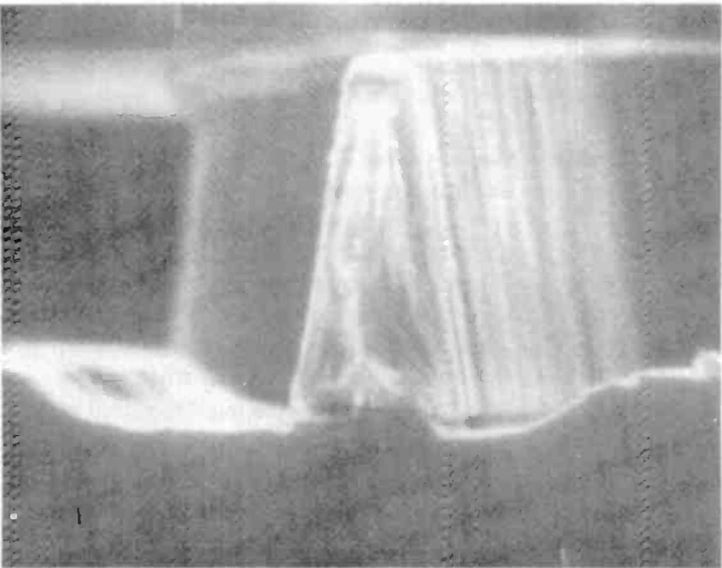
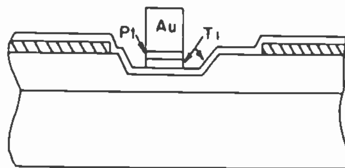
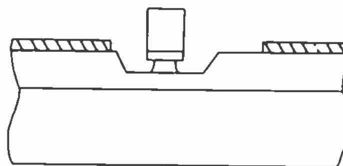


Fig. 5—Cross-sectional view of Ti/Pt/Au-gate looking from the device channel toward the gate pad on wafer B760. Total thickness = 3 μm.



(A) REMOVE PHOTORESIST



(B) CHEMICALLY ETCH TITANIUM

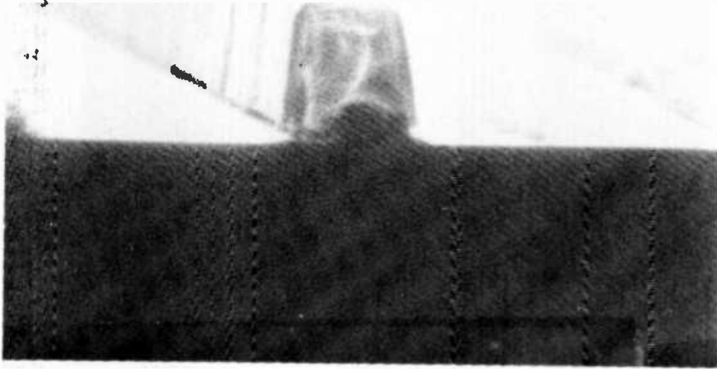
Fig. 6—Production of submicrometer gate length.

uniformity of etching along the line becomes critically important. It is difficult to investigate the etching uniformity simply by looking at the gate cross-section. To observe the degree of raggedness of the etched gate line, the sample was waxed down to a glass substrate, top side down, and all of the GaAs was chemically-etched away without attacking the gate-metal layers. Fig. 8 is an SEM photograph of a section of the gate prepared in this manner. The Ti layer of the gate was etched for a total of 3.25 min. The undercut is quite uniform and demonstrates the good control of the gate length that can be obtained with this technique.

Although good control and reproducibility was obtained with wet chemical etching of the Ti layer of the gate, a study was also made of submicron gates formed by plasma etching. Because the plasma etching characteristics of molybdenum are available in the literature,[7] the gate process outlined above was modified by substituting a molybdenum layer for the Ti layer. The basic lift-off process itself required no modifications. It was found that the plasma etching system did attack gold at a slow rate, so the Mo/Pt/Au gate was capped with a thin layer of Pt before lift-off.

Fig. 9 shows gate cross-sections of a sample with Mo/Pt/Au gates etched for 3.5 and 5.0 minutes, respectively, in an LFE PDS/PDE-301 barrel-type plasma etching system. As can be seen from these photographs, the plasma etching technique also provides good control of the gate length.

(a)



(b)

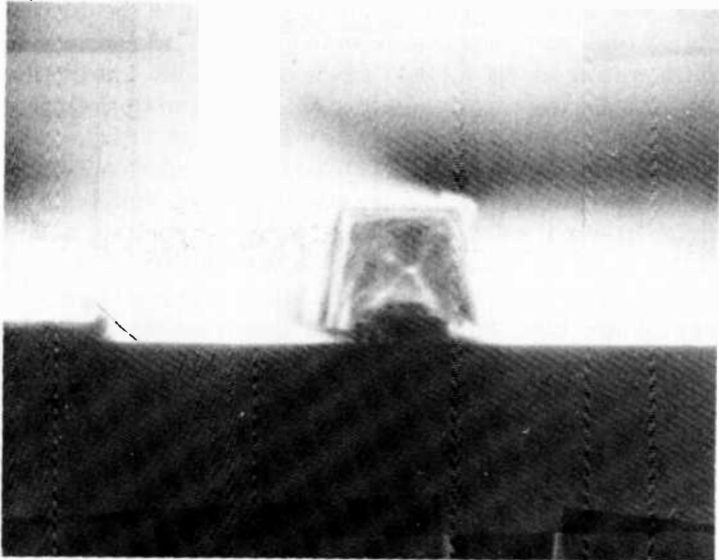


Fig. 7—Cross-section of gate after titanium etching for a total of (a) 1.75 minutes and (b) 3.5 minutes.

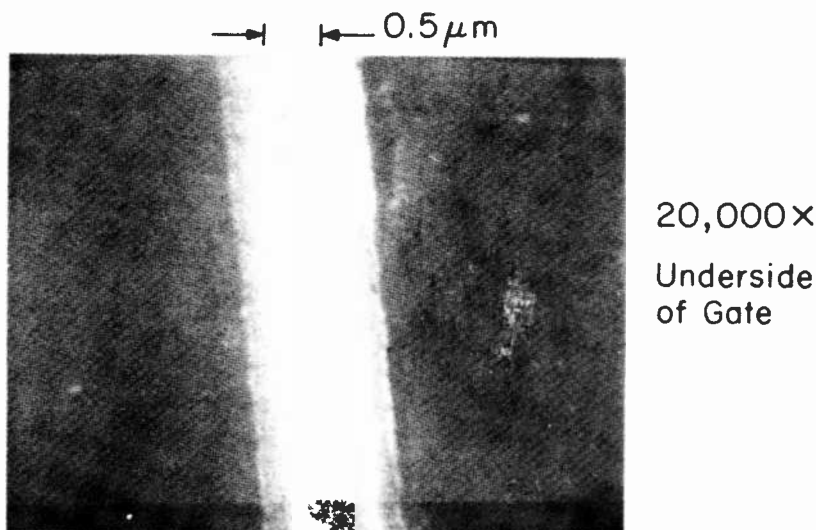


Fig. 8—View of the chemically-etched gate from beneath the gate after etching away all of the GaAs. The Ti etching time for this sample was 3.25 minutes.

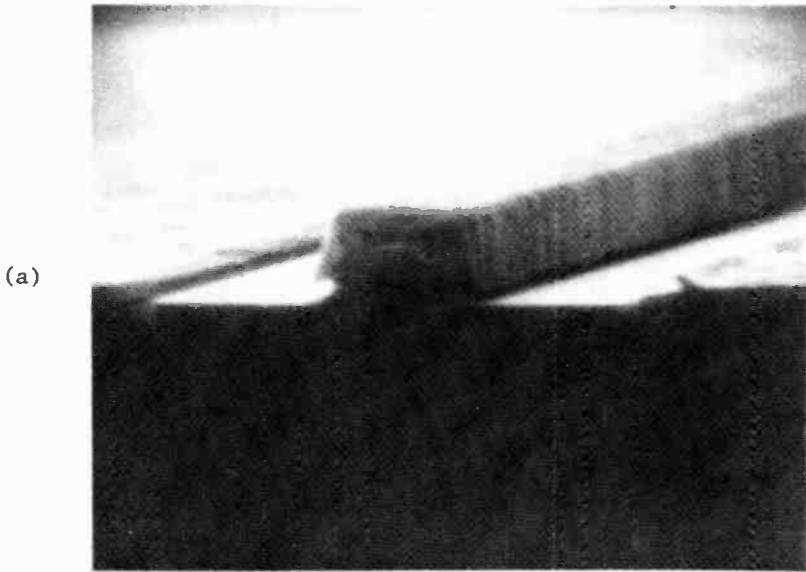
4. Device Performance

The reason for investigating lateral etching and the double-layer photoresist lift-off process has been to produce GaAs power FETs capable of operating above X-band frequencies. Table 1 presents data from power measurements made at or above X-band frequencies for devices whose gates were produced by the methods just described. These results are for a single 600-μm total gate width unit cell that is made up of four 150-μm wide gate stripes connected in parallel. Wafers C44T, D5A, and D37S have active layers produced by ion-implantation of ^{28}Si directly into a semi-insulating Cr-doped GaAs substrate.[8] The active layers of wafers B979, B985, B1271, and B1342 were grown by vapor phase epitaxy. Wafer B985 had an n^+-layer grown on top of the lower doped channel layer. Wafers C44T, D5A, B979, B985, and B1271 had Ti/Pt/Au gate metallization with submicrometer gates formed by wet chemical etching. Wafer B1342 had Mo/Pt/Au gates with the gate length defined by plasma etching of the molybdenum.

5. Conclusions

A technique for producing thick gate metallization with submicrometer gate lengths has been developed to fabricate GaAs power FETs capable of operation at K-band frequencies. This technique employs standard

(a)



(b)

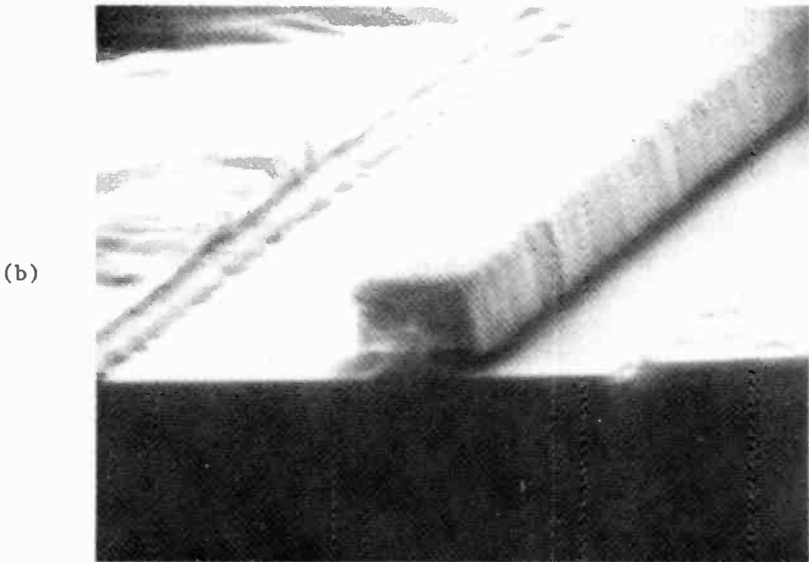


Fig. 9—Cross-section of gate after plasma etching the molybdenum for a total of (a) 3.5 minutes and (b) 5.0 minutes.

Table 1—Power Performance of GaAs FETs as a Function of Frequency (Cell Size = 600 μm Total Gate Width)

Wafer/Device Number	Frequency GHz	Power Gain dB	Output Power mW	Power-Added Efficiency %	Power Out/ Gate Width W/mm
C44T-4	12	6.5	250	29.0	0.44
	15	4.0	240	25.0	0.40
	20	3.9	125	17.7	0.20
	26	3.0	55	5.0	0.09
D5A-4A	11	4.4	276	22.4	0.46
	16.5	3.7	237	18.9	0.40
D5A-7B	16.5	3.7	259	23.6	0.43
B979-7A	16	3.3	350	21	0.58
-9A	24.5	3.3	71	7.4	0.13
B985-4D	11	4.8	300	26	0.50
B1271-Y1	18	3.3	215	14.7	0.40
	20	2.9	196	11	0.33
	22	3.0	99	5.8	0.17
B1342-2	11	4.2	262	19.3	0.44
-5	16.25	3.0	101	10.0	0.17
D37S-80	18	4.4	360	26.8	0.60
-12*	20	3.8	360	21.2	0.30
-2	24	3.6	160	9.1	0.26

* Two cells.

UV contact photolithography and simple wet chemical or plasma etching to achieve submicrometer gate lengths. Development of a T-shaped gate geometry allows submicrometer gate lengths without increasing the gate-metal resistance. GaAs power FET operation was demonstrated at frequencies as high as 26 GHz. An output power of 55 mW with 3-dB power gain (5-dB linear gain) with 5% power-added efficiency was obtained at 26 GHz.

6. Acknowledgment

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GaAs Integrated Circuit Development for Gigabit-Rate Signal Processing

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Abstract—GaAs integrated circuit technology has been developed for gigabit-rate signal processing. The key elements are 1.0-μm gate-length devices, two-level metal interconnections, and dry etching techniques. The test vehicles for the technology development were ring-oscillators, master-slave flipflops, and analog-to-digital converters. These circuits were designed, fabricated, and evaluated. Experimental results of gigahertz-rate operation of GaAs ICs are presented indicating that MSI/LSI circuits can be fabricated to meet specific requirements for gigabit-rate signal processing.

1. Introduction

GaAs MESFETs (metal semiconductor field-effect transistors) have demonstrated 15–18 GHz voltage gain-bandwidth product[1,2] in microwave amplifiers and 34-100 ps propagation delays[3,4] in digital logic circuits. These excellent results are directly attributable to the electronic properties of GaAs. For example, its very high low-field mobility results in smaller series resistance; its low electric field for velocity saturation (7-10 kV/cm) provides lower operating bias; and its semi-insulating property (as a substrate) makes minimum loss interconnections possible between circuits.

We utilized these properties to develop low-power, high-speed medium-scale integrated (MSI) circuits. Our program goals were directed toward (1) developing GaAs-based technology with micrometer size geometries, and (2) designing and fabricating MSI circuits capable of operating at GHz clock rates. We selected (1) standard logic gates and

circuits and (2) comparators for A/Ds as demonstration vehicles. This paper describes GaAs IC design and fabrication procedures that were developed and presents the performance of these ICs at clock rates as high as 1.0 GHz.

2. Design Considerations

In our GaAs IC technology development program, we are concerned with two types of logic elements. The first is the standard NAND, NOR logic gates and the second type is comparators. The design of these logic elements differ in many respects. For example, pinch-off voltage, device current, and signal levels are different in both cases. Therefore, a brief description of the design of these two logic elements is included here.

2.1 Standard NAND, NOR Logic Gates

The parameters of interest in designing logic gates are propagation-delay rise and fall times and power dissipation. For MSI/LSI applications, the power dissipation has to be kept to a minimum and this results in small-geometry devices. When small devices are interconnected, the parasitic capacitances become comparable to the gate input capacitance. Therefore, the parasitic capacitances determine the minimum device size and, hence, the power dissipation. The voltage gain–bandwith product determines the cutoff frequency (f_T) and, hence, the rise and fall times.

2.1.1 Parasitic Capacitance

Parasitic capacitance has two major components, interconnect capacitance (C_i) and fringe capacitance (C_{fr}). From transmission line theory, the interconnect capacitance is given by

$$C_i = 2\pi\epsilon \frac{l}{\ln(7H/W)}$$

where l is the length of the line, W the width of the line, and H the thickness of the substrate.

We will consider interconnect line widths of 2 to 3 μm based on RCA's experience in advanced Si LSI circuits. The circuit yield for such line widths is reasonable. The thickness of the GaAs substrates used is generally between 100 and 120 μm. From the layouts of the circuits being considered, the interconnect lengths are estimated to be about 100 μm. The capacitance of such an interconnect line is calculated to be about 10 fF (1 fF = 10^{-15} F).

The fringing capacitance (C_{fr}) is made up of the interelectrode capacitances between the metal pads. The fringe capacitances that must be considered in the device design are the capacitances (1) between the ohmic pads and the ground plane, (2) between the source-drain pads (C_{sd}), and (3) between the drain-gate pads (C_{dg}). The magnitudes of C_{sd} and C_{dg} depend on the actual FET structures (Pucel, et al.,[5] present a good discussion on this subject). Farrar and Adams[6] have presented calculations of the fringe capacitance between metal pads and ground plane. Each of these components contributes about 1 to 2 pF per centimeter width of the device.

Therefore, the interconnect line capacitance dominates as far as the capacitive loading is considered. The source-drain (C_{sd}) and drain-gate (C_{dg}) capacitances provide feedback paths and affect the gain and stability of the device.

In order for the parasitic capacitances not to influence the circuit performance drastically, the input gate capacitance (C_{sg}) has to be larger than the parasitics. The input gate capacitance is given by

$$C_{sg} = \sqrt{\frac{\epsilon e n}{2V}}\, l_g W,$$

where ϵ = dielectric constant,
e = electronic charge,
n = carrier concentration in the channel,
V = the total reverse bias (including the built-in potential) on the gate,
l_g = gate length, and
W = gate width.

For 1.0-μm long (l_g) gates on 10^{-17} cm^{-3} doped material, the zero bias gate capacitance is about 12 to 15 pF per cm width. For a 15-μm gate-width device, the gate capacitance is 1.5-2.0 times that of the parasitic capacitance. Reducing the device width below 15 μm will reduce power dissipation, but at a sacrifice of speed for 1-μm gate-length devices. Further reduction of device size can be achieved when submicrometer-gate-length devices are used. The fabrication of submicrometer-gate-length devices requires more sophisticated technology.

2.1.2 Switching Speed

The maximum logic switching speed from an active device loaded by the inputs of N similar devices is limited by the ability of the active device to provide the current gain required to drive the N inputs. Consequently, the current gain-bandwidth product determines the upper limit for switching speed. When velocity saturation of the carriers occurs, the cutoff frequency of a FET is given by

$$f_T = \frac{g_m}{2\pi C} = \frac{V_s}{2\pi l_g}.$$

The saturation velocity of electrons in GaAs is about 1.0×10^7 cm/s. For 1.0-μm gate-length devices the cutoff frequency is 15 GHz. This indicates that there is no limitation on the basic device itself. However, the device current must be such that it will be able to charge and discharge the input capacitance of the following gates and the interconnect line capacitances. The charging time (slew time) is given by

$$\Delta T = \frac{C_L \Delta V}{\Delta I},$$

where C_L is the total load capacitance, ΔV the voltage swing from HIGH to LOW or vice-versa, and ΔI the current available for charging or discharging.

For a fan-out of n, $C_L = n(C_{sg} + C_i)$ or $C_L \simeq 1.5n\ C_{sg}$. It was shown earlier that C_{sg} is 12 pF/cm. For a channel pinch-off voltage of 1.5 V, ΔI will be about 0.5 mA/cm. The charging time or slew time is thus 160 ps for a fanout of 2. The propagation delay will be of the same order of magnitude.

2.1.3 Noise Margins

The input-output transfer characteristic of an inverter is shown in Fig. 1. In the transition part of the curve, the voltage gain is given by the ratio

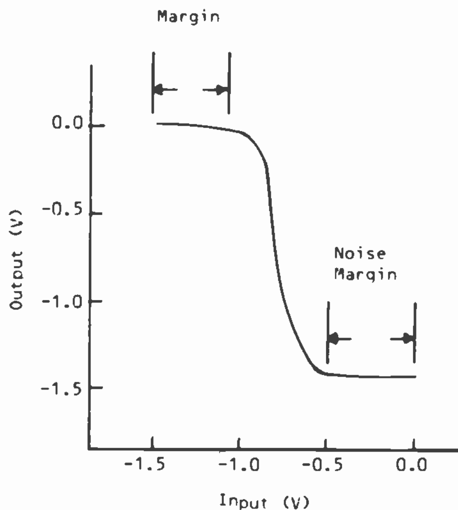

Fig. 1.—Transfer characteristics of an inverter.

of the transconductance of the switching transistor to the transconductance of the load device, which is approximately equal to 2.0. This voltage transition from LOW to HIGH takes place when the current in the switch equals that of the load. Assuming that the drain saturation current of the switch is twice that of the load, the following relation is necessary for the currents in the two transistors to be equal:

$$(1 - \eta_s^{1/2}) = 2(1 - \eta^{1/2}),$$

where $\eta_s = V_B/V_P$ and $\eta = (V_G + V_B)/V_P$. The gate voltage (V_G) required for the transition is given in Table 1 for the different pinch-off voltages (V_p). Here V_G and V_p are normalized to the built-in Schottky-barrier voltage (V_B). The built-in voltage (V_B) is of the order of 0.5 to 0.6 V for Schottky gates fabricated on 10^{17} cm^{-3} dopes GaAs.

For a channel pinch-off voltage of 1.5 V (i.e., $V_p/V_B \approx 3$), Table 1 gives a threshold voltage of about 0.4 V (i.e., $V_G/V_B \simeq 0.86$). The transition from LOW to HIGH will be completed when the gate voltage is $V_p/2$ above the threshold value. As shown in Fig. 1, for input voltages between 0 and −0.4 V, the output stays LOW; for inputs ranging from −0.4 to −1.1 V, a transition region occurs; when the input is −1.1 to −1.5 V, the output is HIGH. Therefore, we have about 0.4 V noise margin for both LOW and HIGH states. Variations in power supply voltages are small (a few mV) and no spurious triggering can occur in digital circuits.

2.1.4 Power Dissipation

The power dissipation in an FET is proportional to (1) the width of the device and (2) the square of the channel pinch-off voltage. A reduction in device width and/or pinch-off voltage results in a corresponding decrease in power dissipation. However, the intrinsic figure of merit ($\sim g_m/2\pi C$) of the FET does not remain constant when the parasitic capacitances approach the value of the gate capacitance. Therefore, the minimum width of the device is fixed from the considerations of the parasitics. Further reduction in power dissipations has to come from a reduction in pinch-off voltage. The FET switches have to be kept fully conducting with a logic "1" input and completely cut off with a logic "0" input. To minimize the excessive gate capacitance, logic "1" should correspond to a voltage level of zero. The logic "0" should

Table 1—Gate Voltage Required for Transition

V_p/V_B	V_G/V_B
2	0.457
3	0.866
4	1.250
5	1.618

correspond to $-V_p$. Thus, the pinch-off voltage essentially determines the logic swing. If the logic swing is too small, false triggering may occur due to noise voltages or fluctuations in the bias voltages. Therefore, the minimum value for pinch-off voltage is set from noise considerations. We must also consider the problem of obtaining GaAs layers suitable for the realization of low pinch-off voltage FETs.

The field-effect transistor operates in a region where the electron velocity is saturated. The current density in the saturation region is given by

$$J_{sat} = neV_{sat},$$

where n is the carrier concentration, e the electron velocity, and V_{sat} the saturation velocity of electrons ($\simeq 10^7$ cm/s for GaAs). The channel thickness (t) can be calculated for a given pinch-off voltage from the relation

$$t = \sqrt{\frac{2\epsilon V_p}{en}}.$$

Due to the depletion under the Schottky gate, the effective channel thickness t' is given by

$$t' = \left(1 - \sqrt{\frac{V_B}{V_p}}\right)t.$$

The drain saturation current (I_{Dsat}) can therefore be written

$$\frac{I_{Dsat}}{W} = \sqrt{2\epsilon neV_p}\; V_{sat}\left(1 - \sqrt{\frac{V_B}{V_p}}\right).$$

For a 1.5-V pinch-off voltage channel and 10^{17} cm^{-3} doped channel,

$$\frac{I_{Dsat}}{W} \simeq 1.0 \text{ A/cm}.$$

The bias voltages required for 1.5 V pinch-off voltage devices are $V_{DD} \simeq 2.5$ V and $V_{SS} \simeq -2.5$ V. Two- or three-level shifting diodes will be required in the inverter. For 15-μm gate width FETs, $I_{Dsat} \simeq 1.0$ mA and the power dissipation will be about 5 to 7.0 mW per inverter.

A 4-input NAND/NOR logic gate is used as a building block, and ring oscillator and master/slave flip-flops are formed by suitably interconnecting several of these gates. The design parameters for a 4-input NAND/NOR gate arc summarized in Table 2.

Table 2—Design Parameters for 4-Input NAND/NOR Gate

Operating Bias $\simeq \pm 2.5$ V
Pinch-off voltage (logic swing) $\simeq 1.5$ V
Power dissipation $\simeq 5$–7 mW
Noise margins = ± 0.4 V
Switching speed (or propagation delay) $\simeq 110$ ps
Width of the switch transistor = 15 μm
Width of the load transistor $\simeq 7.5$–10 μm
Gate length $\simeq 1.0$ μm

2.1.5 Thermal Resistance and Packing Density

If we assume that the interconnect length between adjacent gates is of the order of 100 μm, each inverter occupies about 100×100 μm^2 of the GaAs substrate. We lump the heat generation area of an inverter (including level shifter and source follower) into a 10×5 μm region. Assuming a substrate thickness of 100 μm, the thermal resistance can be estimated (using the curves of Linsted and Surty[7]) to be of the order of 1600°C/W. For a power dissipation of 6.5 mW, the temperature rise is only about 10°C. Thus, a packing density of 100 gates/mm can be achieved without running into thermal limitations.

2.2 Comparators

The principle of operation of GaAs MESFET comparators and the design procedures have been fully discussed in a recent paper by one of the authors.[8] A brief discussion is included here for completeness.

The quantization step (Q) in an A/D is given by

$$Q = \frac{\text{full scale voltage}}{2^n - 1}$$

where n is the number of bits. Full scale voltage is of the order of 1.0–1.5 V. Therefore, for a 2-bit A/D the quantization step is of the order of 0.4–0.5 V. Another consideration in fixing the value of Q is that it should be at least twice the overdrive voltage. Overdrive voltage is the voltage above the threshold value required for the comparator output to make a transition from LOW to HIGH or vice-versa. Overdrive voltage for GaAs MESFET comparators is about 80–100 mV. Hence, the minimum value for Q should be 0.16-0.20 V. A quantized step size of 0.4 V was selected for a 2-bit A/D design.

Three comparators are required for a 2-bit A/D. The least significant bit (LSB) is chosen to be 0.4 V. Therefore, the threshold levels for the comparators are 0.4, 0.8, and 1.2 V. At the threshold value, the transition from "LOW" to HIGH" or "HIGH" to "LOW" takes place at the output of the comparator when the overdrive voltage (ΔV_g) is applied at the

gate. This ΔV_g brings a change in the drain current by ΔI which provides the charging or discharging current for the capacitive load. The load on the comparator is the input capacitance of the source follower and is of the order of 0.03 pF. Therefore, the current required for charging or discharging is given by

$$\Delta I = C\frac{\Delta V}{\Delta t}.$$

The voltage change at the comparator output is of the order of 3 V. For the switching transiton to occur in 150 ps, a current change of 0.6 mA is needed. The size of the switching transistor in the comparator is determined by this current requirement. The change in FET current is given by

$$\Delta I = g_m \Delta V_g,$$

where g_m is the transconductance and ΔV_g is the input voltage swing at the gate. An FET with 6 ms transconductance will bring the 0.6 mA current change for $\Delta_g = 0.1$ V. The minimum size of the switch FET in the comparator is determined from the graphical design procedures described by R. B. Fair.[9] The optimum doping density for FETs is 8–10 $\times 10^{16}$ cm^{-3}. The minimum gate length possible with optical lithography and contact printing is 1.0 μm. The drain saturation current (I_{DSS}) and transconductance, as computed from Figs. 4 and 6 of Fair,[9] are $I_{DSS} = 17.5 - 20$ mA and $g_m = 7.0 - 7.5$ ms for a 100 μm wide device with 5–6 V channel pinch-off voltage. These design parameters are summarized in Table 3. The size of the load transistor is computed from the threshold level for the comparator. At the threshold levels, the switching transistors in the three comparators will have different drain current values and they can be calculated from the relation

$$I_{DS} = I_{DSS}(1 - \eta^{1/2})/(1 - \eta_s^{1/2}),$$

where

I_{DSS} = drain saturation current
$\eta_s = V_B/V_p$, $\eta = (V_B + V_G)/V_p$
V_B = built-in Schottky-barrier voltage
V_G = external gate voltage (threshold voltage level in our case)

Table 3—Design Parameters for FET Comparators

Operating Bias $\simeq$ +7.5 V and −5.0 V
Device Pinch-Off Voltage $\simeq$5.0 V
Switching Speed $\simeq$100–200 ps
Gate Length $\simeq$1.0 μm
Power Dissipation/Comparator = 150–175 mW
Width of the Switching Transistor $\simeq$100 μm

V_p = pinch-off voltage.

The widths of the load transistors for the comparators have been chosen such that their drain saturation currents (I_{DSS}) for $V_G = 0$ equals the saturation currents computed above for different threshold voltage levels. The ratio of the width of the load FET to that of the switch FET for the three comparators is given in Table 4. The Schottky barrier voltage (V_B) and the pinch-off voltage (V_p) are used as parameters.

From Table 4 it is evident that the ratio of the widths is insensitive to the Schottky barrier built-in potential. Since photolithographic techniques allow geometry control to within a micrometer, these comparators are realizable. However, the threshold voltage is more sensitive to the variation in pinch-off voltage and this has to be kept in mind during fabrication.

3. Technology Development

A cross-section of an IC is shown in Fig. 2. It consists of MESFET and Schottky-barrier-diode active elements and two-level metal interconnections. Uniformity of device characteristics, isolation layers with good dielectric properties, and micrometer-size geometry control are the key factors in the technology development for IC fabrication. The need for thin active layers (0.1–0.25 μm) with good electrical properties (e.g., high electron mobility, free of interface traps, etc.) on semi-insulating substrates for realizing operating ICs is obvious and need not be emphasized.

A process schedule developed for the fabrication of GaAs ICs is illustrated in Fig. 3. The starting wafers for IC processing have a thin (0.4–0.6 μm) active layer with $0.8–1.0 \times 10^{17}$ cm^{-3} carrier density on the semi-insulating substrates. The active n-layers are produced by epitaxial growth or ion-implantation and annealing. The majority of the wafers processed in our program were epitaxially grown, although several ion-implanted wafers were also processed recently. There are eight critical steps in GaAs IC fabrication and these are briefly discussed below.

Table 4—Comparator Design Parameters for a 2-Bit A/D

Comparator Threshold	Built-In Voltage	Width of the Load FET/Width of the Switch FET	
		$V_p = 5$ V	$V_p = 6$ V
0.4 V	0.6 V	0.845	0.865
0.8		0.720	0.756
1.2		0.612	0.661
0.4	0.4 V	0.837	0.856
0.8		0.711	0.745
1.2		0.606	0.652

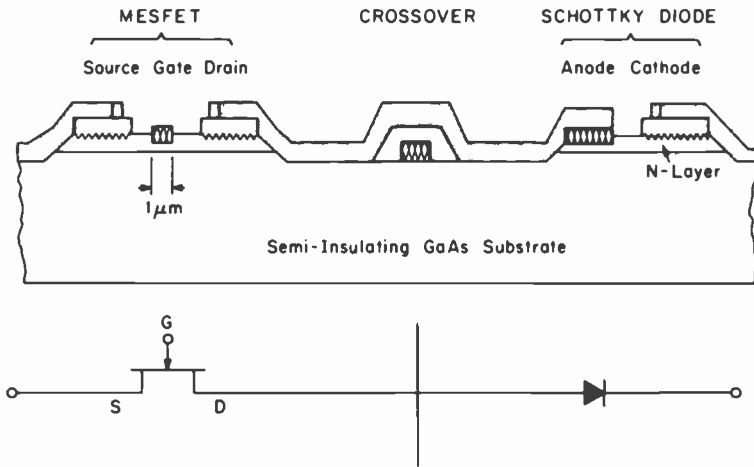

Fig. 2.—GaAs IC cross-section. MESFET and Schottky diode are the active devices. Interconnections with two-level metal lines and dielectric isolation layer for crossovers are also shown.

(*1*) *Electrolytic Thinning:* Unacceptable variations in doping density and thickness can exist in "as received" wafers. These wafers are therefore electrolytically-thinned by anodic oxidation and oxide stripping.[10] This is a self-limiting process and stops when the active layer thickness reaches the maximum breakdown thickness corresponding to the local doping density in any region. Thus, a uniform doping-density-thickness product (*nt*) across the wafer is realized. In the range of doping densities of interest (8×10^{16} to 1.0×10^{17} cm^{-3}), the variation in *nt* of electrolytically-thinned wafers is less than 10%.

(*2*) *Ohmic Contacts:* We use the Au:Ge/Ni/Au system to make ohmic contacts onto the n-layers. These metals are sequentially evaporated onto the wafer. Metal lift-off or the ion-etching technique was used to delineate ohmic contact regions. The metals are then sintered at 420 to 450°C for 1 minute to obtain good ohmic contacts. The specific contact resistance is typically of the order of 2×10^{-5} to 2×10^{-6} ohm cm^2. For the 10×10 μm size contacts on the IC, the ion-etching process yielded much smoother surfaces than metal lift-off.

(*3*) *Device Isolation:* Device isolation is achieved by mesa etching. Due to a low power dissipation requirement, the smallest width of the MESFET used is 7.5 μm. Chemical etching techniques are not suitable for defining such small devices. Therefore, ion etching is used for mesa isolation. The etch rate for GaAs is about 600 Å/min. The end point of etching is determined by measuring either the surface breakdown or the mesa-to-mesa breakdown.

(*4*) *Pinch-Off Voltage Adjustment:* The *nt* product realized using

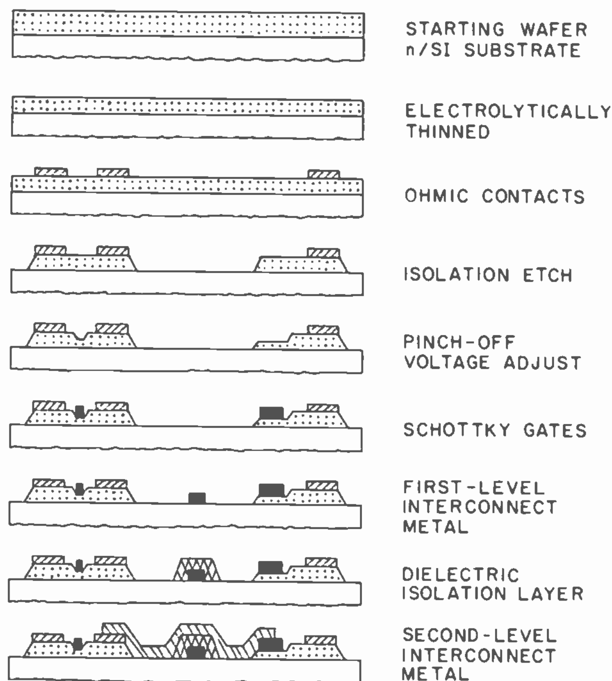

Fig. 3.—Process schedule for IC fabrication. It takes seven masking steps to complete the IC.

electrolytic thinning is about 4×10^{12} cm^{-2} in the desired range of carrier concentration. This results in a channel pinch-off voltage of 10–18 V, which is too high. We have developed a procedure to monitor the open-channel current in test devices on the wafer and selectively etch the channel until the final current is a specific fraction of the open-channel current. This procedure enables the pinch-off voltage for logic-array FETS to be adjusted to about 1.5–2.5 V and that for comparator FETs in the A/D circuit to be adjusted to 5–6 V.

(5) *Schottky Barriers:* Schottky barriers are used in both FET gates and level shifting diodes. We employ either Ti/Pt/Au or Ti/Pd/Au metallization for Schottky barriers. We use a recessed-gate structure for FETs. This reduces the channel resistance between the source-gate and gate-drain regions. Also, this geometry decreases the high electric field in the gate-drain region. The gate regions are defined by means of optical photolithographic techniques. While monitoring the FET channel currents, the gate regions are etched using a touch-up chemical etch. For the level-shifting diodes, the regions under the Schottky contacts may or may not be recessed. Ti/Pt/Au is evaporated using an electron-gun system. Direct lift-off using photoresist is used to define Schottky-barrier

gates. To ensure the continuity of metal across the mesa edges, a total metal thickness of 3000–4000 Å is used.

The *I-V* characteristics measured on discrete test FETs are shown in Fig. 4. The current saturation voltage (V_{Dsat}) is about 1.2 V for the recessed gate structure and 2.0 V for the planar structure.

(6) *Dielectric-Isolation Layers:* Two-level metal interconnections are required for GaAs ICs. Dielectric layers are used for isolation in defining the crossovers. In the early program phase, we used plasma-deposited Si_3N_4 as the isolation layer. The composition of the Si_3N_4 varied from run to run, and thus the etch rates were different. This resulted in severe undercutting of the isolation islands, making it difficult to define small Si_3N_4 islands for crossovers. The step coverage of the Si_3N_4 on mesa edges was poor. It appears that this is an inherent problem and silicon oxynitride must be used to obtain better step coverage. Therefore, we investigated polyimide as an alternative. Dupont PI-2555 polyimide with 3:1 dilution by weight in pyrolydinone was found to be excellent for isolation layers on GaAs ICs. This polyimide requires low-temperature curing (~200°C) and can be patterned by either oxygen plasma or chemical etching. Both these processes are compatible with our GaAs IC fabrication process. The smallest isolation islands defined in this program are of the order of 7.5 × 10.0 μm.

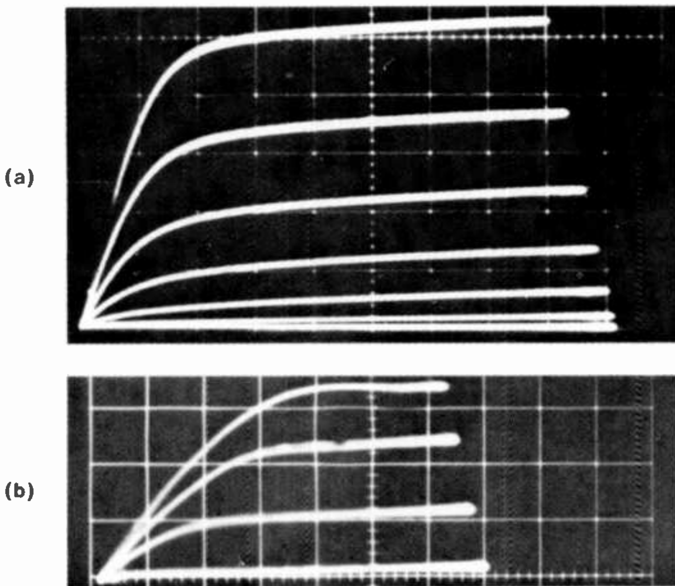

Fig. 4.—Current-voltage characterstics of test FETs: (a) recessed gate device and (b) uniform channel device. (Vertical scale is 0.2 mA/div.; horizontal 0.5 V/div.; 0.5 V/step.)

(7) *Interconnections:* Two-level interconnections are required to complete the GaAs ICs. In order to carry the desired currents, particularly in the bias lines, a metal thickness of the order of 0.7 to 1.0 μm should be used. The minimum width of the interconnect (signal) lines in 3 μm. Defining thick interconnect metal lines using contact printing and lift-off was difficult. Procedures were developed using a 1.5–1.7 μm thick photoresist and chlorobenzene soak for defining the interconnect pattern. Ti/Pd/Au or Ti/Pt/Au metal systems were used for interconnections. Fig. 5 shows a typical two-level interconnect pattern with a polyimide isolation. The first-level metal line is about 3.0 μm wide.

(8) *GaAs Integrated Circuits:* We have fabricated three types of ICs: (1) ring oscillators, (2) type-D or R-S master/slave flip-flops, and (3) 2-bit analog-to-digital converts. Fig. 6 shows photomicrographs of the three types of GaAs ICs. The chip size is 0.65 × 0.450 mm for the logic arrays and 1.3 × 1.0 mm for the A/D converter. 1.0-μm-gate-length FETs are used in A/D ICs and 1.5-μm-gate-length dual-gate FETs are used in ring oscillators and D flip-flop ICs. The width of the smallest (constant current load) FET is 7.5 μm.

4. Experimental Results

4.1 Logic Gates

Inverters

DC transfer characteristics and response to sine-wave input were measured on test inverters. A typical dc transfer characteristic of an inverter

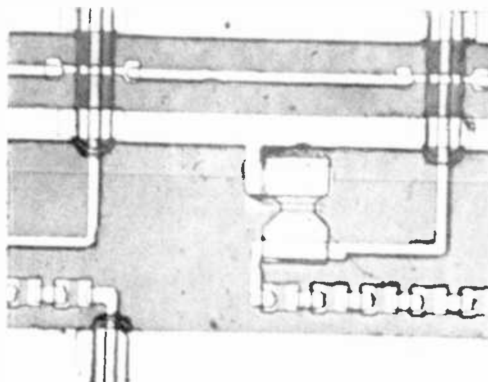

Fig. 5.—Photomicrograph of a two-level interconnect pattern. Polyimide dielectric layer used for isolating crossovers. The width of the smallest line is 3.0 μm. Polyimide islands as small as 7.5–10 μm were used.

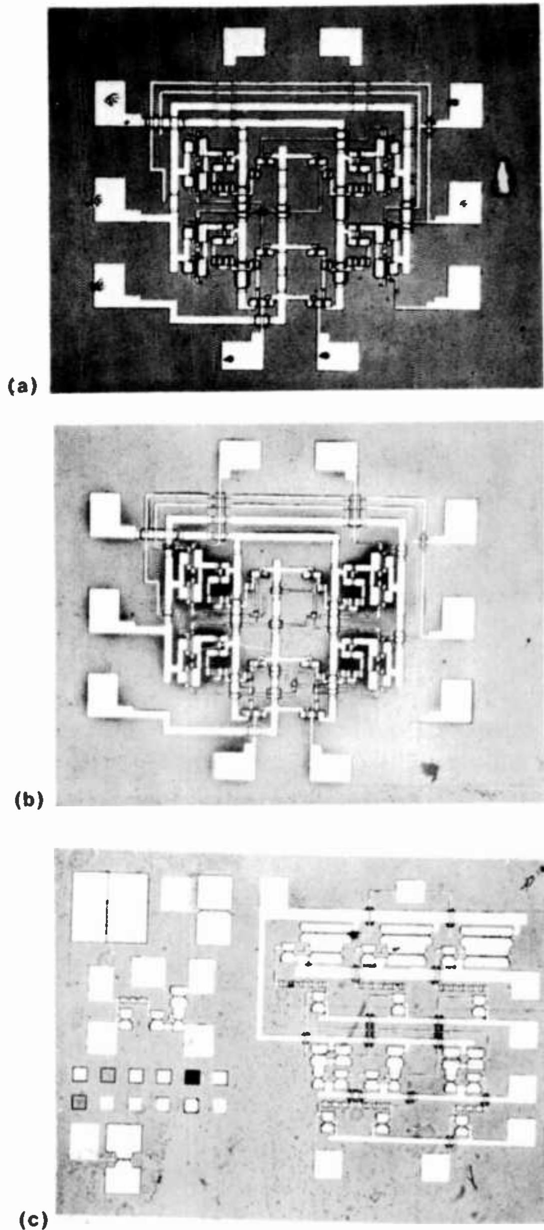

Fig. 6.—Photomicrographs of GaAs ICs: (a) ring-oscillator, fan-in = 2, fan-out = 2; (b) D-type master/slave flip-flop; and (c) 2-bit A/D converter. 1.0-μm gate-length devices used in A/D and 1.5-μm gate-length devices used in ring oscillators and flip-flops.

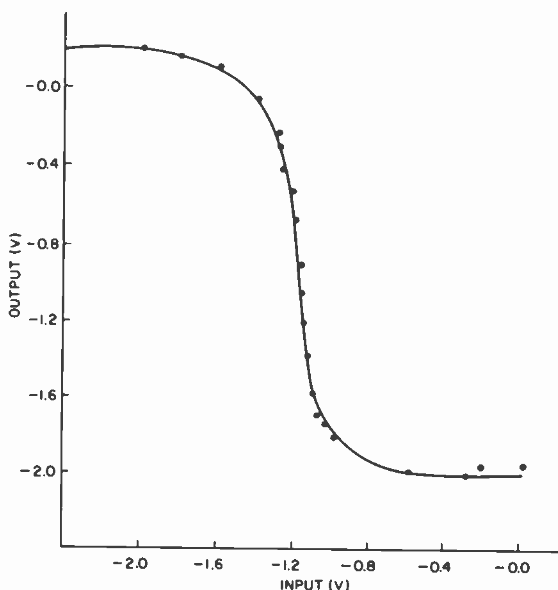

Fig. 7.—DC transfer characteristics of an inverter. The noise margins for both LOW and HIGH are about 1.0 V.

is shown in Fig. 7. The channel pinch-off voltage is about 2.5 V for this device. The transition from LOW to HIGH or vice-versa occurs at about 1.2 V and the noise margins are about 0.5–1.0 V. These results are in close agreement with the design values. The response of the inverter for a 950 MHz sine wave input signal as measured on a probe station is shown in Fig. 8. A 100:1 attenuator directly soldered to the tungsten probe mounted in a micromanipulator was used for the output probe in this

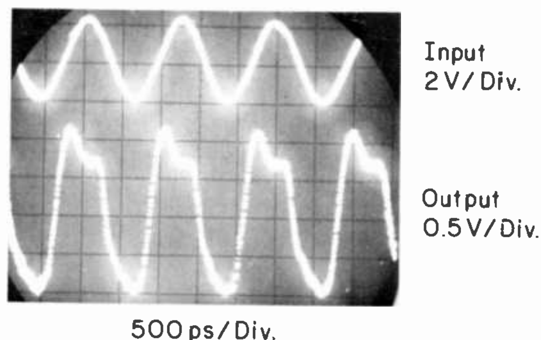

Fig. 8.—Response of an inverter to a 950 MHz sine wave input signal. Sharpening of the rise and fall times can be seen in the output pulse.

measurement. The measurements can be further extended if the attentuators are defined on the IC itself.

Ring Oscillators

Ring oscillator circuits are used to determine the propagation delay and dc dissipation per logic gate. Many of the results reported in the literature are for a fan-out of 1. In practical circuits, a fan-out of 2 or more is desired. We therefore used a ring oscillator circuit with a fan-in of 2 and a fan-out of 2 in our experiments. The ring oscillator output frequency was measured on a spectrum analyzer and also identified using a frequency meter. The circuits operated at bias voltages as low as +3.0 V and −2.5 V for V_{DD} and V_{SS}, respectively. Ring oscillator frequency increased with an increase in bias voltage. Circuits operated satisfactorily at bias voltages as high as +5.0 V and −4.5 V. The lowest and highest oscillating frequencies were 675 and 910 MHz. The corresponding propagation delays were 210 and 170 ps with 7.0 and 9.5 mW power dissipation. The delay-dissipation product was 1.4–1.6 pJ. It is important to note that 1.5 μm gate-length FETs were used in these circuits and also that the second gates of the dual-gate MESFETs were connected to form the ring. These results are plotted on the propagation delay and power dissipation chart shown in Fig. 9. Our results (marked with an asterisk) are in good agreement with published data on GaAs (TTL or BFL) cir-

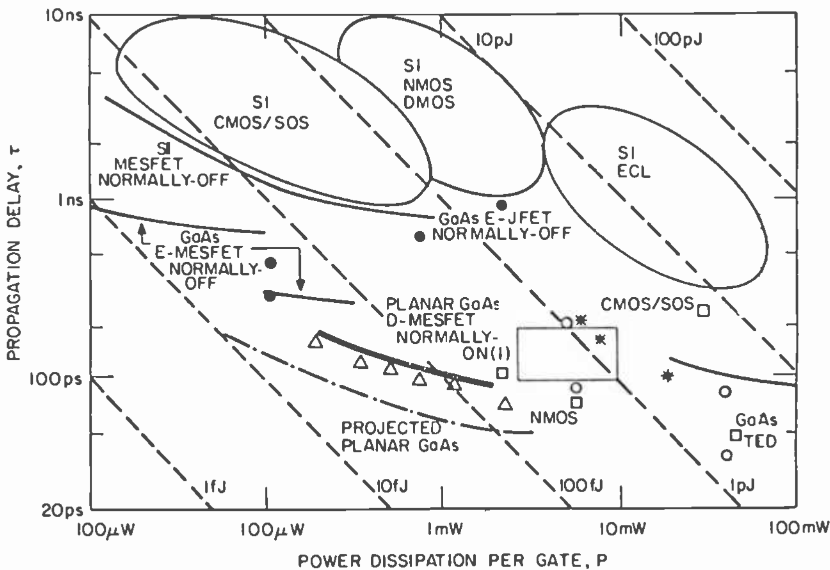

Fig. 9.—Speed-power performance chart for various IC technologies. Published data on GaAs buffered FET logic devices are shown by the box. Our experimental results are shown by an asterisk.

cuits and with our design goals. Based on these results, we can confidently project a 100–120 ps delay when 1.0 μm gate-length devices are used.

R-S Flip-Flops

To evaluate the R-S flip-flops, we needed CLOCK, $\overline{\text{CLOCK}}$, R and S inputs. It was difficult to provide these four-input signals at 1.0 GHz clock frequency and minimize the signal feedthrough and cross talk. The R-S flip-flops were only tested up to 100 MHz. However, these flip-flops have been externally connected as divide-by-two or divide-by-four circuits. The divide-by-four circuit operated satisfactorily up to an input frequency of 280 MHz. The parasitics due to the bonding pads and output measuring probe limited the performance. We are trying to improve our probe system to facilitate measurements into the GHz region. The input-output waveforms of these divide circuits are shown in Fig. 10.

4.2 A/D Converters

The A/D IC consists of the comparators and the coding logic. Sample and hold circuits and the digital-to-analog (D/A) circuits are not incorporated on the chip. Such circuits operating at 1.0 GHz sampling rates

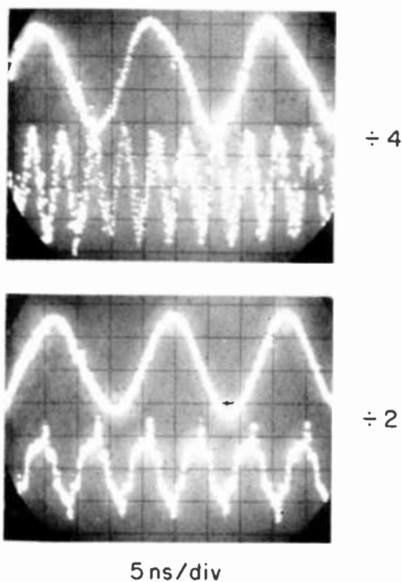

Fig. 10.—Performance of divide-by-two and divide-by-four circuits. D-flip-flops were externally interconnected to form divide circuits. Divide-by-four circuits operated at 280 MHz. Parasitics due to external bonding connections and reflections at discontinuities in the probe station limited the test frequency range.

are not available. Therefore, the IC was tested in the following way. DC biases were optimized separately for the comparator and logic circuits. A variable input (0 to −1.2 V) was fed to the comparators and the corresponding binary coded outputs (2^1 and 2^0 bits) were monitored. The performance of the ICs was then studied from dc through GHz sampling rates. Fig. 11 shows the performance of the 2-bit A/D for a dc input voltage. Successful operation of the threshold comparators and the coding logic is clearly demonstrated in this figure. The two-bit A/D converter was tested with input pulses as small as 0.5–0.8 ns wide. Such an input pulse corresponds to the sample-and-hold pulse that the comparators see. The response of the circuit for a 0.5 ns wide sample-and-hold type input is shown in Fig. 12. The sampling rate is the highest reported in the literature for devices operating at room temperature. These results clearly demonstrate the feasibility of GaAs A/D monolithic ICs for GHz sampling rate operation. However, further studies should be carried out to determine the offset errors, linearity errors, and quantization errors before it can be incorporated into any real system. Also, with the present architecture, the resolution of this type of A/D is limited to 3 or 4 bits.

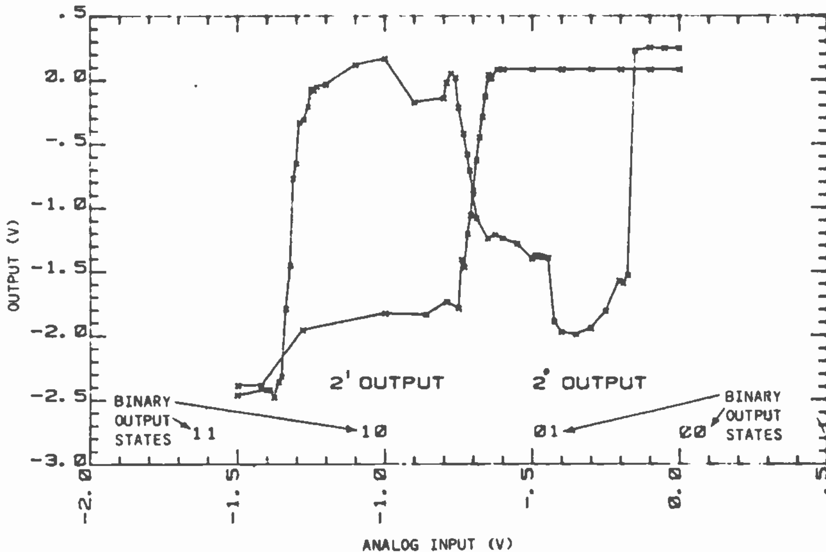

Fig. 11.—Response of the 2-bit A/D for dc input.

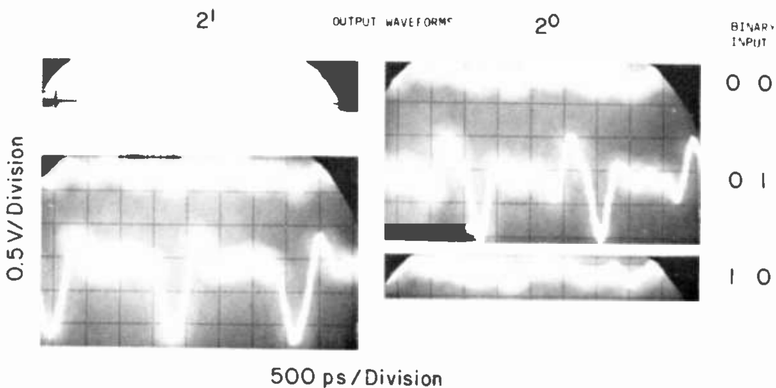

Fig. 12.—Response of the 2-bit A/D for a 0.5-ns wide sample-and-hold type input.

5. Conclusions

GaAs MSI technology has been developed and several types of ICs have been designed, fabricated and evaluated. The potential of GaAs-based integrated circuits for multigigabit-rate logic applications has been demonstrated. Pseudorandom code generators, programmable divide-by-5/6 counters, and 3- bit A/D circuits are being developed for possible system applications. Other ICs with the same complexity can be easily implemented with our present technology.

Acknowledgments

The authors would like to express appreciation to Dr. F. Sterzer for his interest and support in this work and to Dr. S. Y. Narayan for many discussions and critical reading of the manuscript. Thanks are also due Dr. W. R. Curtice for analyzing some of the circuits on the computer and to Messrs. S. T. Jolly, D. Capewell, and Ms. E. E. Beck for providing GaAs wafers. The masks for 2-bit A/D were generated by R. Geshner, R. Greening, and J. Mitchell of the RCA Solid State Division.

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$Ga_{0.47}In_{0.53}As$ Metal Insulator Field-Effect Transistors (MISFETs) for Microwave Frequency Applications

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Abstract—This paper describes the fabrication and characteristics of $Ga_{0.47}In_{0.53}As$ MISFETSs. The devices were fabricated on vapor-phase epitaxial n^+/n $Ga_{0.47}In_{0.53}As$ layers lattice matched to Fe-doped, semi-insulating InP substrates and used chemically vapor-deposited SiO_2 as the gate insulator.

MISFETS with 3-μm gate length have given gains of 4 dB at 6 GHz with a power output of 57 mW and power-added efficiency of 19.7%. Capacitance voltage and conductance voltage measurements show that the SiO_2 ternary interface is well behaved with interface state densities of 2.5×10^{12} cm^{-2} eV^{-1} to 2×10^{10} cm^{-2} eV^{-1} at gate biases for -2 V to $+5$ V (inversion to accumulation) and little oxide trapping as evidenced by minimal C-V hysteresis. Effective mobilities (μ_{eff}) as high as 5200 cm^2 V^{-1} s^{-1} have been measured, considerably higher than those reported for InP or GaInAsP quaternary MISFETs.

1. Introduction

The need for higher-operating-frequency field-effect transistors (FET) has prompted the investigation of $Ga_{0.47}In_{0.53}As$ lattice matched to semi-insulating InP as the semiconductor material for such applications. Theoretical and experimental studies have shown that $Ga_{0.47}In_{0.53}As$ lattice matched to Fe-doped semi-insulating InP substrates has the potential advantages of higher low-field electron mobility and peak electron drift velocity over GaAs.[1-3] However, this lattice matched ternary has a relatively low bandgap (0.72–0.75 eV), resulting in a Schottky barrier height for typical metals of 0.3 eV.[4] This low Schottky barrier height presents problems in fabricating Schottky barrier gate FETs

(MESFETs). Various approaches to circumvent this problem, including use of p^+n junction gates[5] and heterojunction gates[6] are being investigated in many laboratories. In the present work, we have taken the approach of developing metal-insulator-semiconductor field-effect transistors (MISFETs) with $Ga_{0.47}In_{0.53}As$.

Recent advances in vapor phase epitaxial growth of ternary layers have provided $Ga_{0.47}In_{0.53}As$ material of excellent surface morphology, complex doping profiles, excellent lattice match to Fe-doped semi-insulating (SI) InP, and having high low-field electron mobilities.[7] This material has been used to fabricate ternary MISFETs having an all-epitaxial n^+/n semi-insulating InP structure.

These devices have shown excellent depletion and enhancement characteristics, and 3-μm gate length MISFETs have given 4-dB gain at 6 GHz with a power out of 57 mW and 19.7% power-added efficiency.

Initial investigation of the SiO_2/ternary interface have shown interface state densities of about 2.5×10^{12} cm^{-2} eV^{-1} to 2×10^{10} cm^{-2} eV^{-1} with time constants of 1–100 μs. Effective mobilities of 5200 cm^2 V^{-1} s^{-1} have been measured, considerably greater than those reported for InP and GaInAsP quaternary MISFETs.[8,9]

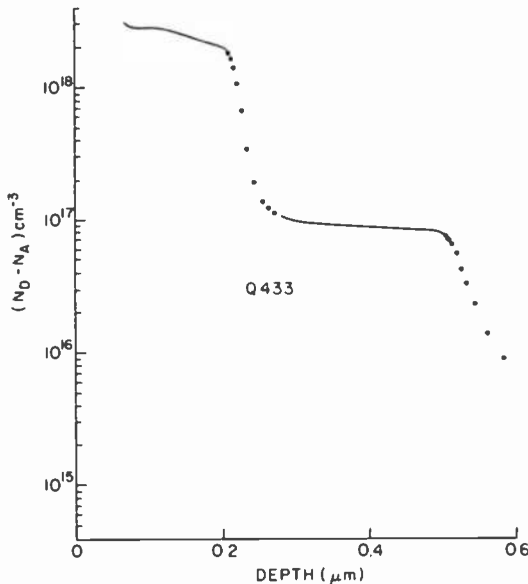

Fig. 1—Carrier profile of ternary wafer Q433.

2. Device Fabrication

$Ga_{0.47}In_{0.53}As$ ternary layers were grown on Fe-doped semi-insulating InP substrates with ⟨100⟩ orientation, using the hydride vapor-phase epitaxial growth technique. The structure used is $n^+/n/SI$ InP having a typical doping profile as shown in Fig. 1. The n^+ region is about 0.2 μm thick, doped to $2\text{–}3 \times 10^{18}$ cm^{-3}, and the n-layer is about 0.3 μm thick, doped to 1×10^{17} cm^{-3}. These starting wafers have excellent surface morphology, and the doping profile is quite uniform over the wafer. The lattice mismatch on the wafers was less than 0.1%.[7]

The process steps employed in fabricating $Ga_{0.47}In_{0.53}As$ ternary MISFETs (hereinafter called ternary MISFETs) are outlined in Fig. 2. Source and drain ohmic contacts are formed by evaporating an AuGe/Ni/Au layer over the wafer and defining the source and drains by photoresist lift-off. The devices are isolated by etching away the n^+/n layer forming mesas (Fig. 2c). Then the channel is formed by etching a "notch" through the n^+ region and into the n-layer until the desired drain current is achieved (Fig. 2d). SiO_2, typically 1000 Å thick, is then chemically vapor deposited at 350°C. This SiO_2 layer is the gate insulator and is a critical step in achieving good MISFET characteristics (Fig. 2e). Next, Ti/Pt/Au metallization is evaporated and defined to form the gate electrode. The gate is aligned over the channel notch and overlaps the n^+ region at the edges of the notch (Fig. 2f). Finally, the SiO_2 over the source and drain ohmic contacts is removed, completing the device processing.

The finished ternary MISFETs have a gate length of about 2.5 μm, with four gate stripes of 150-μm width in parallel. Fig. 3 is a photograph of the completed device. On the same mask set there is a FATFET device for diagnostic measurements on the SiO_2/ternary interface. This device has a gate length of 140 μm and a gate width of 240 μm, providing sufficient gate capacitance for capitance-voltage and other diagnostic measurements.

3. Experimental Results

A curve tracer display of a typical $Ga_{0.47}In_{0.53}As$ MISFET $I\text{–}V$ characteristic is shown in Fig. 4. This device, from wafer Q463, has a gate length l of about 3 μm, a gate width of 600 μm, and a SiO_2 thickness of ~1000 Å.

The right trace in the photograph shows the $I\text{–}V$ characteristics with negative gate bias applied. The device has a transconductance of about 15 mS at zero gate bias and pinches off at about −4 V. The left trace shows the characteristics with positive gate bias, showing excellent en-

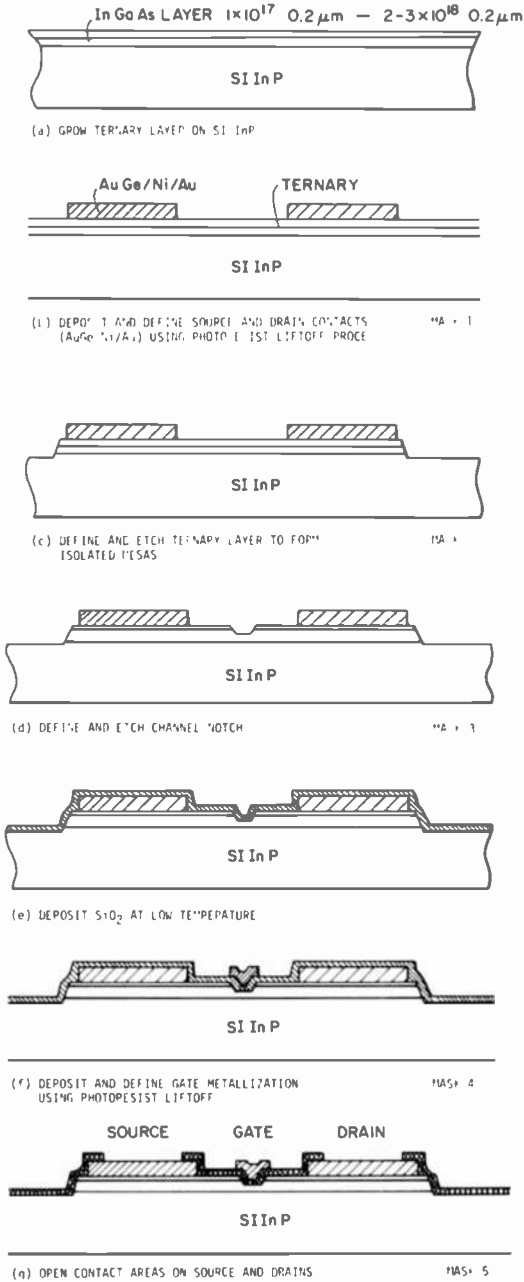

Fig. 2—GaInAs/InP ternary MISFET process sequence.

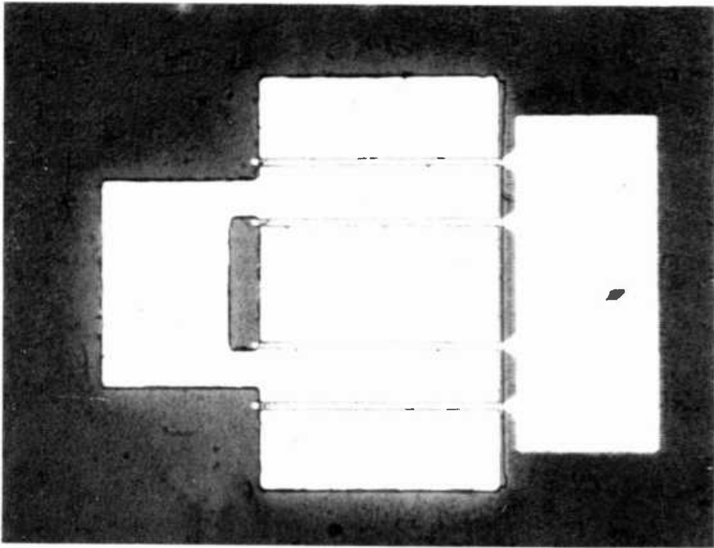

Fig. 3—Completed $Ga_{0.47}In_{0.53}As$ MISFET.

hancement with the transconductance being maintained at 15 mS until over 3-V positive bias is applied to the gate. The knee voltage is quite low, indicating low source and drain resistances. The photograph shows some "looping" in the characteristics. This looping is indicative of hysteresis in the capacitance versus voltage curves and will be discussed

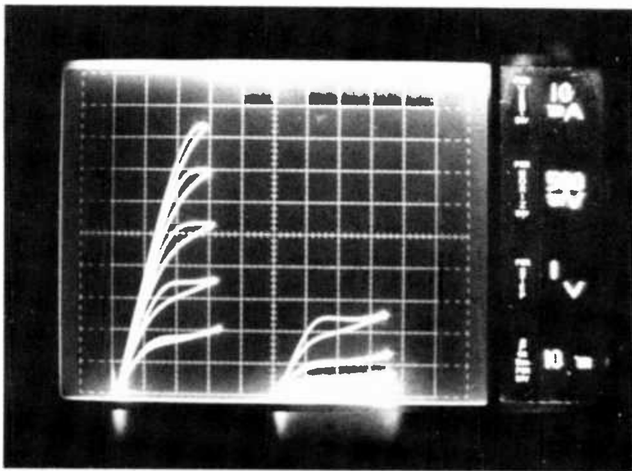

Fig. 4—Drain-source characteristics of wafer Q463 quasi-full gate structure.

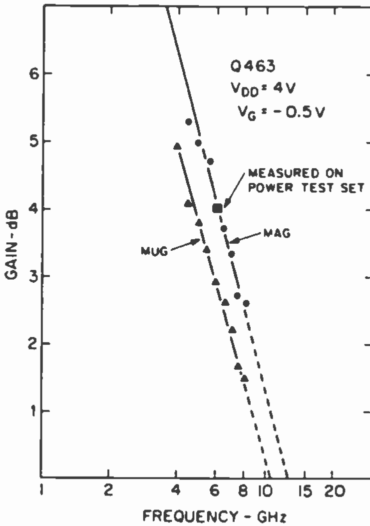

Fig. 5—MAG and MUG calculated from S-parameter measurements for MISFET from wafer Q463.

later. It can be reduced significantly by proper annealing of the oxide-ternary interface.

RF measurements were made on other devices from the same wafer (Q463). These devices had less than optimum drain current, typical zero gate-bias current being 80 mA instead of the 200 mA desired for a 600-μm wide device.

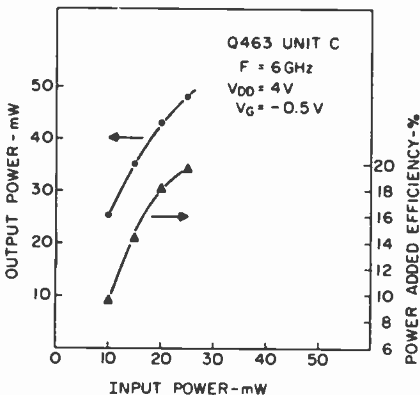

Fig. 6—Measured power output and power-added efficiency for device from wafer Q463.

Fig. 5 is a plot of maximum available gain (MAG) and the maximum unilateral gain (MUG) calculated from S-parameters measured on a network analyzer. Also shown on the plot is the small signal gain of the device measured on a power test set. It is evident that at 6 GHz, the measured small-signal gain and the MAG computed from S-parameters agree very well. It should be noted that the gain roll-off is less than 6 dB/octave. This is also observed in GaAs FETs where we usually observe a less than 6 dB/octave roll-off followed by a greater than 6 dB/octave roll-off at some critical frequency.

Fig. 6 is a plot of output power and power-added efficiency as a function of input power for the same device. These data were measured at 6 GHz with a drain voltage of 4 V. The power output is low due to the low zero-bias device drain current and the low drain voltage used. For this device geometry, the small-signal gain is also lower than optimum because of the less than optimum zero-gate-bias drain current. However, under the above conditions, the power-added efficiency, given by

$$\eta = \frac{P_{out} - P_{in}}{P_{dc}},$$

is quite reasonable, reaching 19.7%.

As expected, there was little change in gain as the gate bias was varied about zero volts. For devices from wafer Q463, the maximum gain was achieved with a small signal negative gate bias of −0.3 to −0.5 V, with the gain varying only by about 0.2 dB for a ±0.5 V variation of gate bias.

As previously mentioned, a large test MISFET is included on the mask

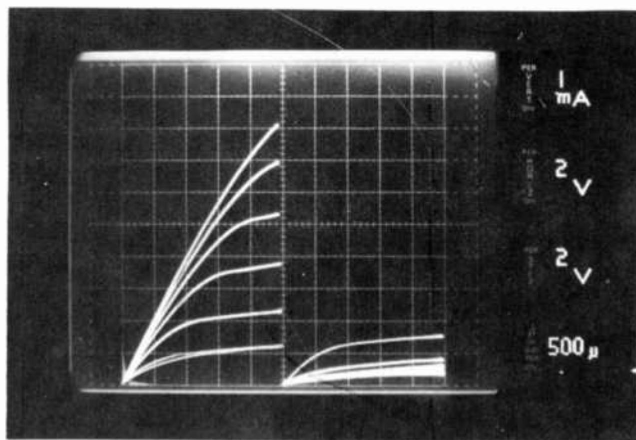

Fig. 7—Drain characteristics of ternary wafer Q228 FATFET geometry (gate length 140 μm, gate width 240 μm). Left trace at positive gate bias and right trace with negative gate bias.

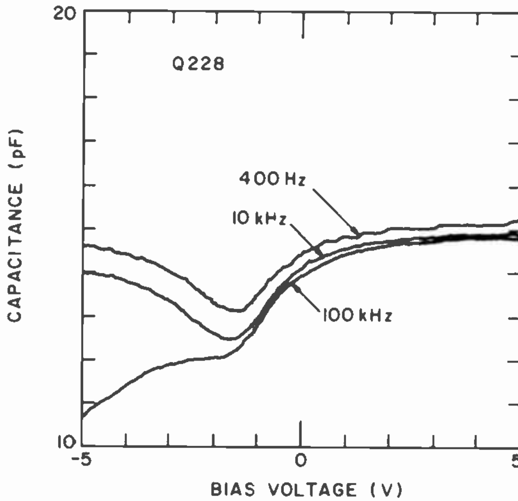

Fig. 8—Capacitance versus voltage at various frequencies (wafer Q228 FATFET).

set. This FATFET device has sufficiently large gate capacitance for capacitance-voltage measurements to be made on the device itself.

Fig. 7 is a photograph of the *I–V* characteristics of a FATFET device from wafer Q228. Drain current enhancement with positive gate voltage is shown on the left trace. The right trace shows incomplete pinch-off

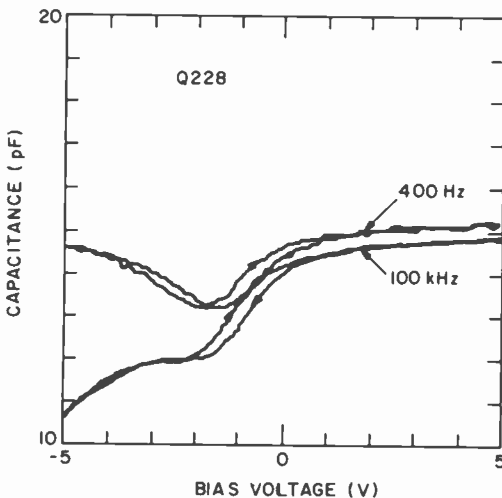

Fig. 9—Capacitance versus voltage at various frequencies (wafer Q228 FATFET) with bias swept positive to negative and back to positive.

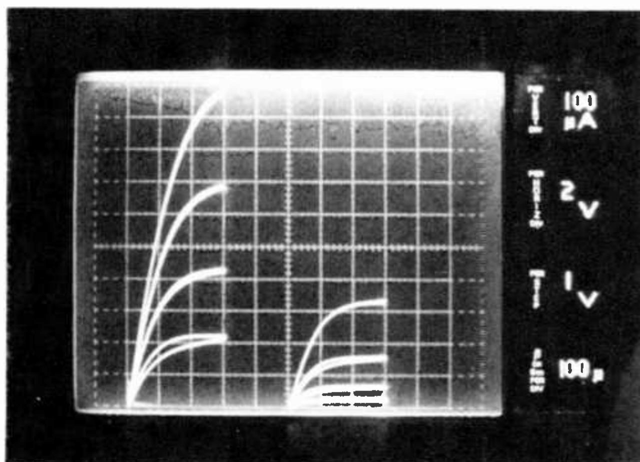

Fig. 10—*I–V* characteristics of FATFET from wafer Q463. Left trace at positive gate bias and right trace negative gate bias.

with negative gate bias, which is due, in this case, to the gate not completely overlapping the area between source and drain, leaving a parallel non-gate-controlled current path between source and drain.

From the device geometry and n-layer doping and thickness, the drain current for this device was computed to be 2.2 mA, which is in reasonable agreement with the measured value of 1.5 mA. The large enhanced drain current with positive gate bias is believed to be due to electron accumulation at the semiconductor surface, i.e., the fermi level is not pinned at mid-gap, which is very unlike the case for GaAs MIS devices.

It should be noted that the traces in Fig. 7 show very little looping, indicating little hysteresis in the capacitance voltage characteristics.

Fig. 8 is a capacitance versus voltage plot at three frequencies for a FATFET from wafer Q228. Note that the dispersion with frequency is small and that the typical deep depletion characteristic is seen at 100 kHz. Fig. 9 is a capacitance versus voltage plot at two frequencies with the bias voltage swept from positive to negative and back to positive. The hysteresis is small ($\simeq$0.3 V) and is independent of frequency.

Fig. 10 shows the *I–V* characteristics of a FATFET from wafer Q463. This device has the channel notch etched quite deeply so that the n-layer was removed to nearly the doping tail at the n-GaInAs/SI InP interface resulting in an n-layer with low doping density. Hence the zero-bias drain current is quite low, as can be seen in the photograph.

Fig. 11 is the capacitance-voltage curve of this device taken at various frequencies. The large C_{MAX} to C_{MIN} ratio is indicative of the low doping

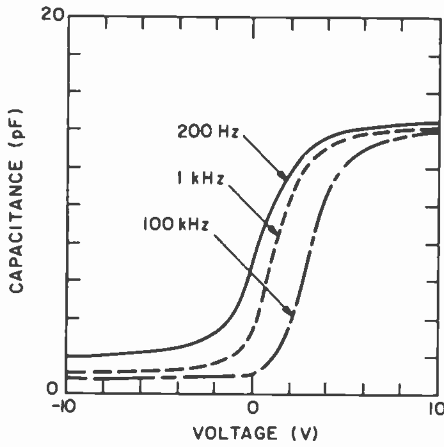

Fig. 11—Capacitance versus voltage at various frequencies (wafer Q463 FATFET).

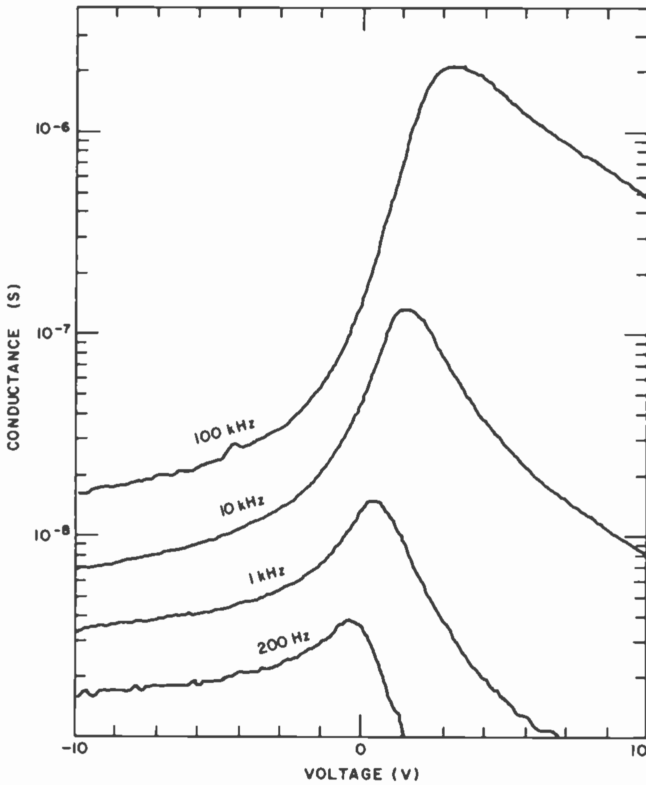

Fig. 12—Conductance versus voltage plots at various frequencies (wafer Q463 FATFET).

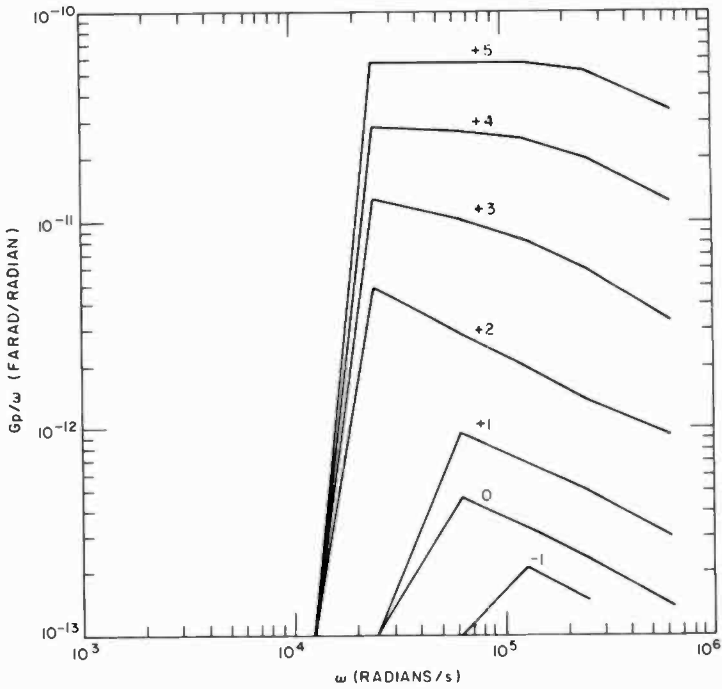

Fig. 13—Equivalent parallel conductance/ω versus ω at different gate voltages (wafer Q463 FATFET).

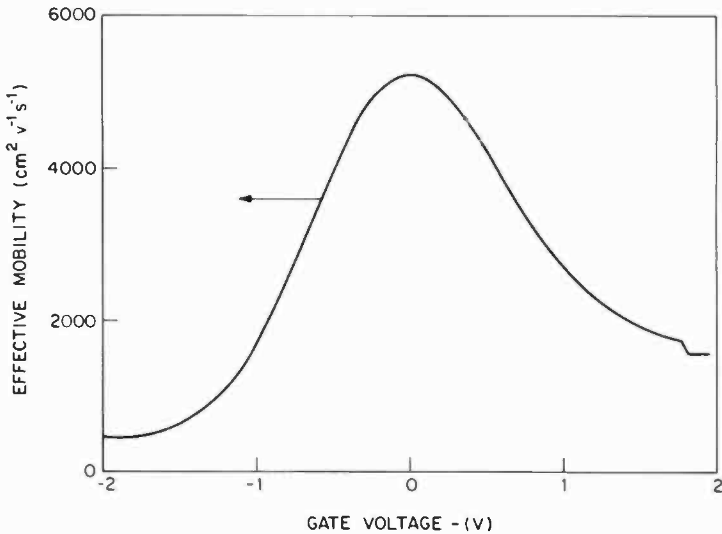

Fig. 14—Effective mobility versus gate voltage (wafer Q463 FATFET).

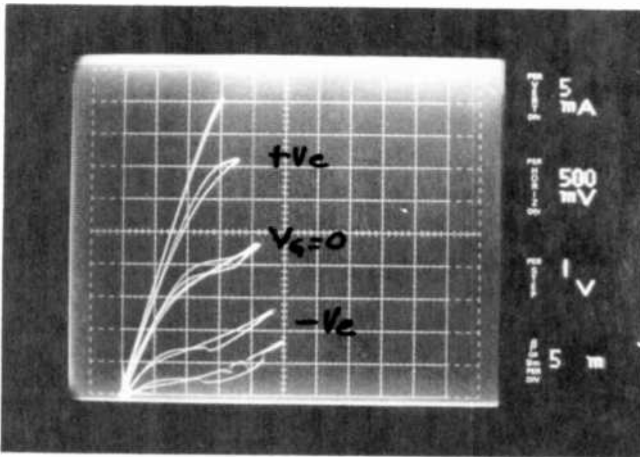

Fig. 15—Drain-source characteristics of wafer Q228 quasi-full gate structure (gate length ~ 3.5 μm, gate width ~600 μm).

density. These C–V curves are typical of the SiO_2/ternary system and although they show some dispersion, the results are quite good.

Fig. 12 shows the conductance versus voltage at various frequencies for the same device. The conductance peak moves to more positive voltages as the frequency is increased, as normally occurs. Again, these results are quite typical of the SiO_2/ternary system.

Fig. 13 shows the equivalent parallel conductance (G_p) divided by ω *versus* ω for various bias voltages. These measurements were made using rather wide, discrete frequency steps dictated by the instrumentation. However, it can be seen that G_p/ω peaks quite broadly, indicating a spectrum of interface state time constants. These data indicate that the interface state density ranges from $\sim 2.5 \times 10^{12}$ cm^{-2} eV^{-1} with the +5 V on the gate to $\sim 2 \times 10^{10}$ cm^{-2} eV^{-1} at −1 V on the gate. These interface state levels are quite reasonable for a MIS system, and we believe that they can be further improved. The time constants of the states are in the range of 1–100 μs.

A very important parameter in MIS devices is the effective field-effect mobility μ_{eff}. At small values of V, this is given by the expression;

$$\mu_{eff} = \frac{L}{W}\frac{1}{C_i}\frac{g_m}{V_D},$$

where L = gate length
W = gate width
V_D = drain voltage
C_i = gate capacitance/unit area
g_m = transconductance

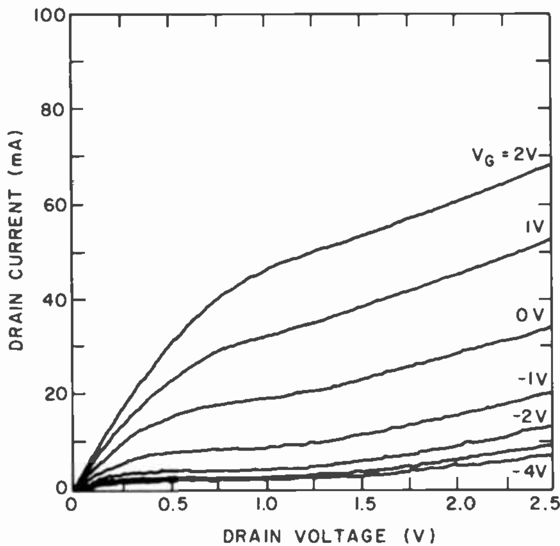

Fig. 16—Source-drain dc *I–V* characteristics of a typical device from wafer Q228.

This effective mobility is always lower than the channel bulk mobility because the measurement depends on modulating the channel current with the gate. Hence, interface states, oxide traps, and surface scattering, which reduce the effective channel modulation, result in a lower mobility value.

Fig. 14 is a plot of effective mobility as a function of gate voltage for the same FATFET device. The mobility peak is 5200 $cm^2 V^{-1} s^{-1}$ for this device. This value compares with the value of the order of 800 $cm^2 V^{-1} s^{-1}$ typical for silicon MOS devices, 1850 $cm^2 V^{-1} s^{-1}$ for InP MISFETs reported by Lile, et al,[8] and 2300 $cm^2 V^{-1} s^{-1}$ for $Ga_xIn_{1-x}As_yP_{1-y}$ quaternary MISFETs reported by Shinoda and Kobayashi.[9]

An important consideration in III–V compound MISFETs has been the degradation in the device response at frequencies below 100 Hz caused by very high densities of interface states. Messick[10] showed that InP devices fabricated in his laboratory were little degraded at dc compared to GaAs MISFETs.

Fig. 15 shows the *I–V* characteristics, displayed on a curve tracer, at 120 Hz of a device from wafer Q228. Fig. 16 shows the quasi-dc *I–V* characteristics of the same devices. These characteristics were measured on a computer-controlled system which increments the drain current in small steps until a set drain voltage is reached at a fixed gate bias. The process is repeated for various gate bias. The 120-Hz characteristics showed a g_m of ~10 mS at zero gate bias, and the quasi-dc characteristics

also showed a g_m of ~10 mS. This shows that the low frequency response of the ternary MISFETs is not degraded significantly as is indicated by the reasonable interface state densities achieved.

4. Conclusions

We have developed a technology for the fabrication of MISFET devices on $Ga_{0.47}In_{0.53}As$ lattice-matched to Fe-doped InP semi-insulating substrates.

Ternary MISFET devices with gate length of 3 μm have been fabricated and have demonstrated 4 dB gain at 6 GHz with power-added efficiency of 19.7% at 57 mW power output. Other devices have achieved power outputs of 75 mW at 6 GHz.

Capacitance-voltage and conductance-voltage measurements have shown that the SiO_2 ternary interface showed interface state densities of the order of 1×10^{12} cm^{-2} eV^{-1} with little oxide trapping, and measurements of μ_{eff} have given values as high as 5200 cm^2 V^{-1} s^{-1}, considerably higher than values reported for InP or GaInAsP quaternary MISFET devices.

Further improvements in device performance are possible by reducing gate length. With a reasonably-behaved SiO_2 ternary interface, ternary MISFETs hold promise for exploiting the high drift mobility and peak drift velocity achievable in $Ga_{0.47}In_{0.53}As$.

Acknowledgments

The authors are indebted to F. Sterzer for his encouragement and support of this work, to R. Camisa for making rf device measurements, and to J. Cordas and E. Mykietyn who assembled the devices.

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Lumped-Element GaAs FET Power Amplifiers

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Abstract—Very small (1.5 × 2.25 mm) lumped-element matched amplifiers have been developed that cover the 6–12 GHz band with 0.3-W and 0.6-W minimum output levels. Using these matched carriers as building blocks, a 6–11 GHz, 1-W, two-stage amplifier and a 7–12 GHz, 1-W, four-stage amplifier have been demonstrated.

1. Introduction

The size of broadband microwave components can be significantly reduced without degradation in performance by using lumped-element as opposed to distributed matching networks. In fact, when package parasitics become part of the network topology, superior performance is possible. In power amplifier arrays that use matched passive combiners, the small amplifier size also results in high combining efficiency[1] because the losses associated with extraneous line lengths between amplifiers are eliminated.

Earlier work on microwave lumped-element circuits concentrated on biopolar transistor amplifiers and filter networks.[2] Recently, lumped-element techniques have been applied to substrate-grounded[3] and to flip-chip[4] GaAs power FETs. Previous work on flip-chips has been reported on narrow-band 10-W performance in X-band. In this paper, a broadband lumped-element topology is described that uses commercially-available flip-chip power FETs. A unique feature of this circuit is that individual elements within the network can be experimentally optimized using a special test fixture. This approach, coupled with

computer-aided measurement and design methods, has resulted in the realization of broadband FET power amplifiers.

Very small (1.5 × 2.25 mm) matched carriers have been developed that achieve minimum output power levels of 0.3 W and 0.6W over the 6–12 GHz frequency band. Using these small amplifiers as building blocks, broadband power amplifiers have been demonstrated. Amplifiers have been built at the 1-W output power level that cover the 6–11 GHz and the 7–12 GHz bands. Broader bandwidths and higher power extensions of this work are possible and are currently in progress.

2. Lumped-Element Amplifier Techniques

Many synthesis and computer-aided-design procedures are available for the design of amplifiers using lumped-element or distributed networks. The models predict the salient physical characteristics of the circuit, but means for handling modeling errors and perturbations in element values should also be provided for in the design. This paper describes a broadband power amplifier model that allows for accessible measurement points within the network topology. First, a lumped-element circuit approach is outlined, including the amplifier circuit model and its practical realization. The experimental techniques developed for probing and optimizing this circuit topology are then described. Last, details of specific amplifier designs are presented.

Fig. 1 is a mathematical model for a single-stage, lumped-element amplifier, including input matching network, device and package, and output matching network. Fig. 2 shows the circuit corresponding to the proposed model. The matching circuit, which consists of two inductors and one capacitor on each side of the transistor, is in a discrete hybrid form. The inductors are 12.5-μm thick gold ribbons with widths from 75–125 μm and lengths varying as required. The capacitors are parallel-plate chip capacitors, which can be purchased commercially or fab-

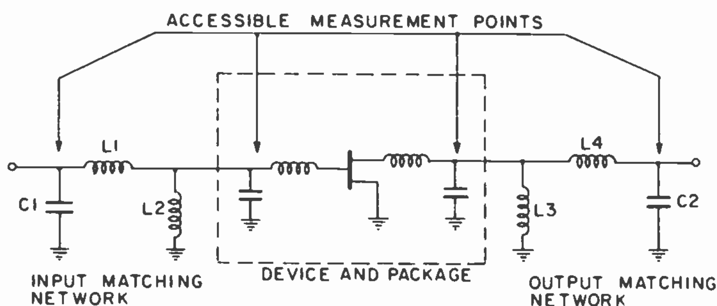

Fig. 1—Lumped-element amplifier topology.

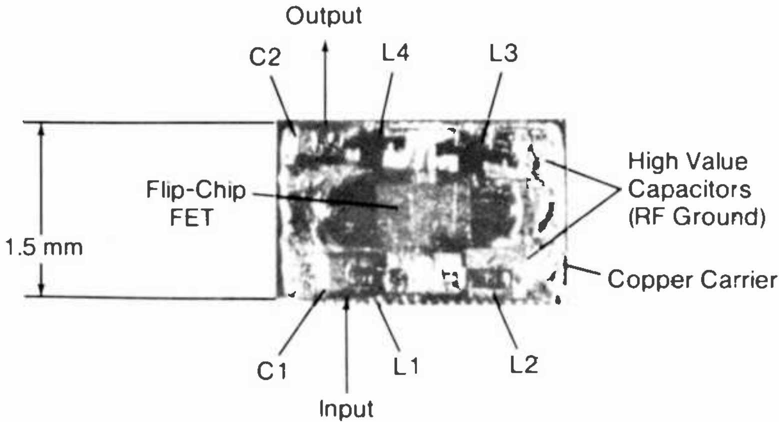

Fig. 2—Lumped-element amplifier.

ricated from high dielectric constant ceramics such as rutile. The shunt inductors (L_2, L_3) are realized by using high value (10–20 pF) capacitors that act as rf grounds and that can also be used for bias injection. The devices used are commercially-available 1200-μm and 2400-μm gate-width GaAs power transistors (MSC 88102 and MSC 88104 devices.*)

The circuit layout is such that all capacitors are mounted on either the input or output edge of the carrier, which makes them accessible measurements points. A special pressure contacting fixture was developed to probe the circuit at these points, as shown in Fig. 3. This fixture consists of an input (gate) and output (drain) rf connector and a center flange (source) with a groove for the device carrier. The center conductor of each connector makes contact to a capacitor while at the same time pushing the device carrier into the center flange. Since the lumped-element amplifier is not soldered into the test fixture, optimization of the circuit can be accomplished without exposing the devices to unnecessary temperature cycling. The ability to demount the circuit from the fixture many times without damaging the device is particularly useful during the initial stages of circuit development.

This approach has proven to be very low loss and is limited only by the rf connector used. Accurate, low-loss measurements are achieved because possible sources of measurement error are reduced to within a connector length. The present fixture uses a Cablewave† hermetic connector that has a low VSWR characteristic through 18 GHz. Newer connectors are presently in development for use through 34 GHz. Fixture

* Microwave Semiconductor Corp., Somerset, N.J. 08873
† Cablewave Systems, Inc., 60 Dodge Ave., North Haven, Conn. 06473

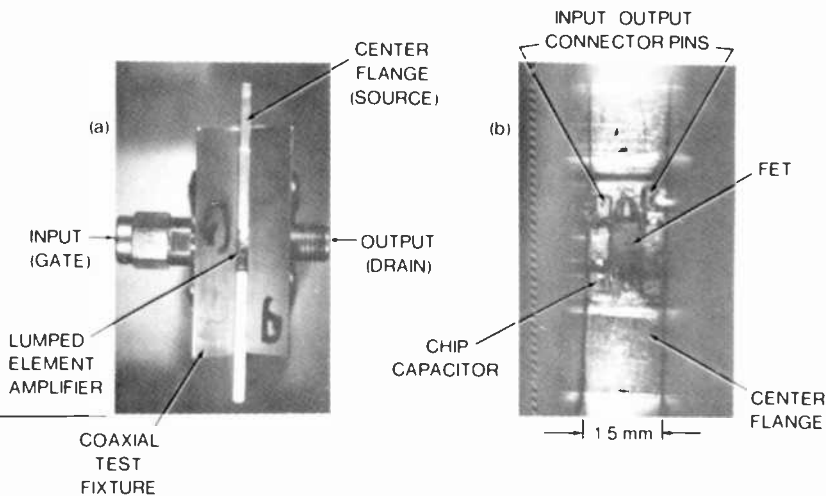

Fig. 3—Lumped-element amplifier coaxial test fixture (left) and FET mounting detail (right).

losses are also minimized by preventing higher order modes from propagating and by avoiding spurious responses. This is accomplished by creating a waveguide-below-cutoff cavity in the center plate of the fixture that allows only TEM modes to propagate.

3. Device Characterization

Both small-signal and large-signal measurements can be made using the coaxial test fixture. Typically, an accurate set of S parameters is obtained and then an input network is designed and implemented. Once the input is matched, the output impedance for maximum output power is determined for different input power levels. The best-fit output network is then synthesized in order to approximate the experimentally-determined load contour. One or two iterations in this procedure are usually required to optimize the input and output network. Going through a complete design cycle can be time consuming, but both large and small signal design optimization can be performed for lumped-element amplifiers using the approach described here.

3.1 Small-Signal ($\bar{S}$ Parameters)

The small-signal properties of a device alone can be characterized by placing the coaxial center pins on the gate and drain standoffs without connecting any of the other elements in Fig. 1. Obtaining an accurate

set of $\bar{S}$ parameters is usually difficult at this point because of the low input impedances on the gate side of a power FET.

The measurement problem becomes more critical at microwave frequencies for large (>2.4 mm) gate width devices. One way to circumvent this is to correct the measured data for fixture errors. It is always desirable, however, to start with the best $\bar{S}$ parameters possible. In Fig. 4, S_{11} and S_{22} for both MSC 88102 (1200 μm) and MSC 88104 (2400 μm) devices are plotted from 6–12 GHz. These measurements are not corrected for errors introduced by the fixture. The reference plane for this data is at the edge of the device carrier, which is obtained by calibrating outside the device fixture and then subtracting out connector lengths, which are assumed lossless. These uncorrected measurements are very well behaved and were subsequently used directly for amplifier design.

As is indicated in Fig. 4, the device input and output package parasitics are each modeled as a single section, low-pass network. These measurements indicate that the input for both the 1200-μm and 2400-μm devices typically behaves as a series resonant circuit with an approximate real part of 6 Ω and 4 Ω, respectively. The series resonance is a result of the device capacitance resonating with the wire bonds from the chip to

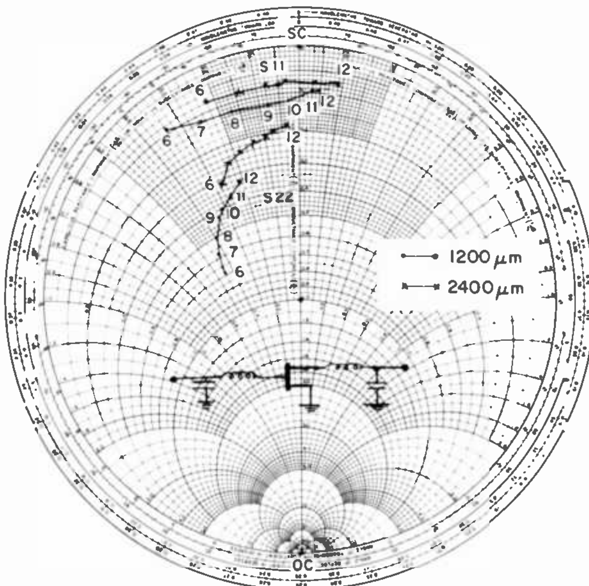

Fig. 4—6–12 GHz small-signal S_{11} and S_{22} plots for MSC 88102 (1200 μm) and MSC 88104 (2400 μm) devices.

the carrier standoff. The output impedance similarly acts essentially as a parallel resonant circuit with an additional series inductance.

3.2 Large Signal (Load/Pull)

In the same coaxial test fixture, matched, lumped-element amplifiers are tested and optimized under large-signal conditions. Of particular interest is the output load impedance for maximum output power or maximum efficiency. In Fig. 5, the large-signal load impedance and the associated performance for various input drive conditions are summarized for an MSC 88102 device at 12 GHz. The data was generated by using a computer assisted loadpull measurement technique developed by Dr. F. Sechi and R. Paglione of our laboratory. Each impedance point corresponds to the load impedance at a given input power for maximum power-added efficiency. Table 1 gives the output power, dc power dissipation, gain, and drain current associated with each measurement point in Fig. 5. Fig. 5 also shows the small-signal load termination point, which is different from the impedances for large-signal conditions. Fig. 6 shows the same type data from 13–16 GHz with a constant input drive level of 200 mW.

4. 6–12 Matched Carriers

Both 1200-μm width (MSC 88102) and 2400-μm width (MSC 88104)

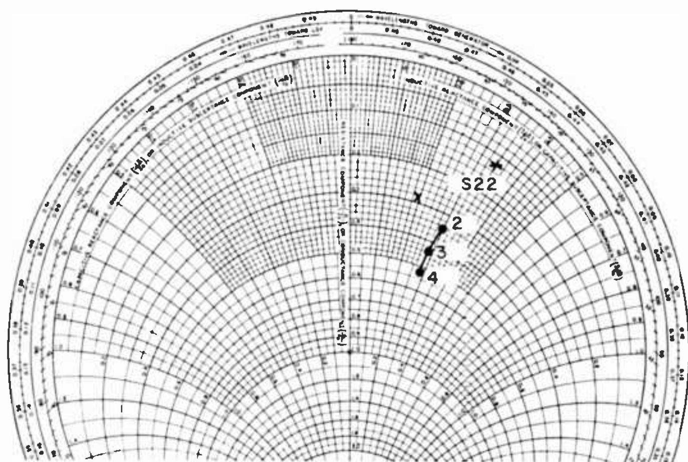

Fig. 5—12 GHz load/pull test for MSC 88102 device versus input power (see Table 1 for circuit values for points).

Table 1—Input Power, Output Power, DC Power Dissipation, Gain and Drain Current for Impedance Points in Fig. 5.

Point	P_i (W)	P_o (W)	Diss. (W)	Eff. (%)	G (dB)	I (mA)
2	0.09	0.30	0.74	21.4	4.99	0.12
3	0.14	0.41	0.79	25.2	4.61	0.13
4	0.19	0.45	0.83	23.2	3.61	0.13

power FETs have been matched over the 6–12 GHz frequency range. In this section, details of each design are presented, including element values and performance. The gain, power, and efficiency numbers presented were measured at the carrier level using the coaxial test fixture previously described. The devices are operated with external bias networks that are commercially available; the losses associated with these circuits are not included in the measurements.

4.1 1200-μm Gate-Width Design

Using a lumped-element design approach, an MSC 88102 device was matched over the full 6–12 GHz frequency range. Fig. 7 outlines the circuit topology, including individual element values; Table 2 gives values

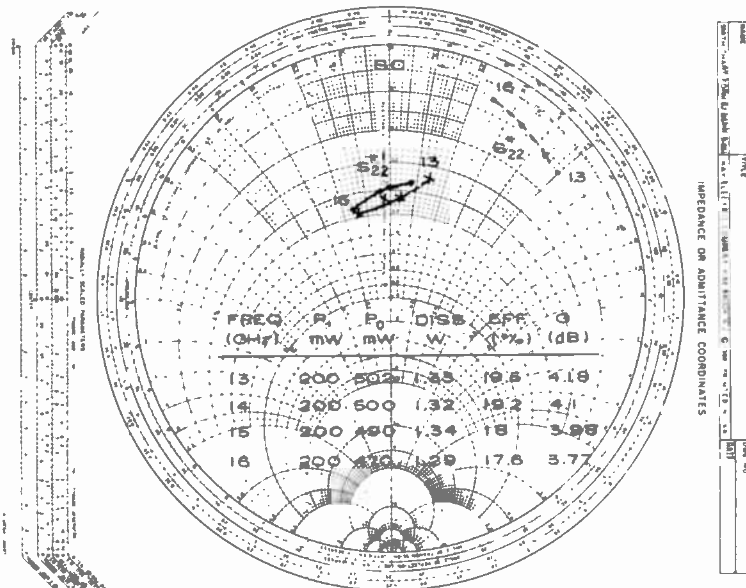

Fig. 6—13–16 GHz load/pull test for MSC 88102 device for an input power of 200 mW.

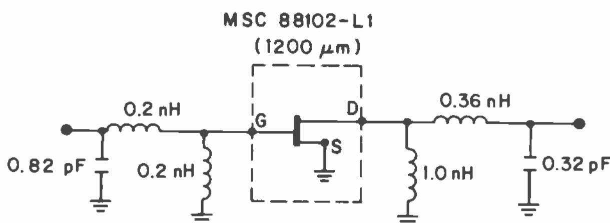

Fig. 7—Circuit topology for MSC 88102 matched carrier design, including element values (values for simulated performance are given in Table 2).

for the simulated small-signal performance. In the initial stages of development, gain flatness was not a primary concern; as a result, no attempt was made to decrease the high gain response at the lower end of the frequency band where the intrinsic transistor gain is much higher. In this design, the capacitors are parallel-plate ATC (American Technical Ceramics) capacitors that are premeasured before assembly into the circuit. The lumped-element inductors are gold ribbons that are welded onto the capacitors. The larger value inductor (1 nH) is obtained by looping the ribbon. High value capacitors (15–22 pF) are used to rf ground the shunt inductors in the topology. Figs. 8 and 9 compare the simulated and measured performance of the input and output matching networks. The correlation between the simulated and measured impedance for both the input and output is good.

In this design, the high and low ends of the band are matched and the middle is compromised. In many devices that have been matched, this tradeoff is always present; as will be seen later, it becomes more serious for the larger 2400-μm-width MSC 88104. The major effects of the high S_{11} reflection coefficient in the center of the band are decreased gain and efficiency. Fig. 10 shows the gain and power-added efficiency measured for the simulated device (MSC 88102). In this plot, the gain and efficiency are maximum at the band extremes and both have a 50% decrease in the center of the measured band. The efficiency is 17.5% at the high

Table 2 Simulated Value for Small-Signal Performance Obtained Using Circuit Topology in Fig. 7.

FREQ	S_{11}, I.RC X	1.000*	S_{22}, O.RC X	1.000*	F_{GAIN} PH X	1.000DB
6.00	.831	76.73	.627	−53.16	9.257	171.08
7.000	.240	−56.79	.432	−140.61	10.148	91.01
8.000	.436	−153.76	.302	−161.83	8.381	42.13
9.000	.443	156.49	.281	−173.80	6.887	.74
10.000	.356	117.98	.306	171.54	6.757	−33.48
11.000	.419	21.56	.258	122.95	6.780	−79.73
12.000	.542	−43.25	.258	62.86	5.803	−117.10

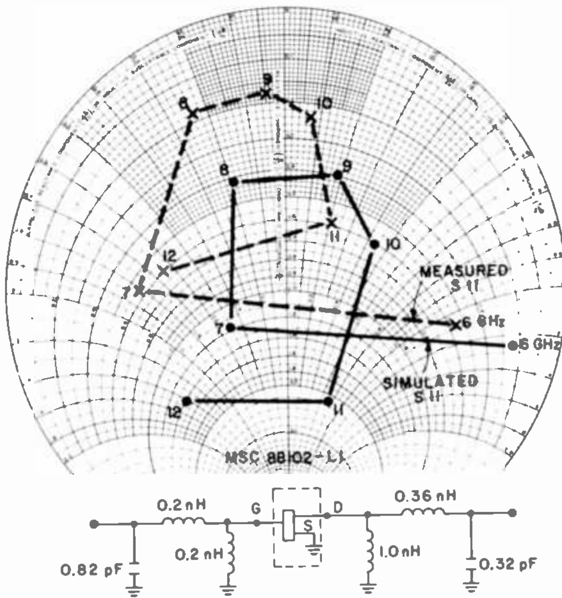

Fig. 8—Simulated and measured S_{11} coefficient for MSC 88102.

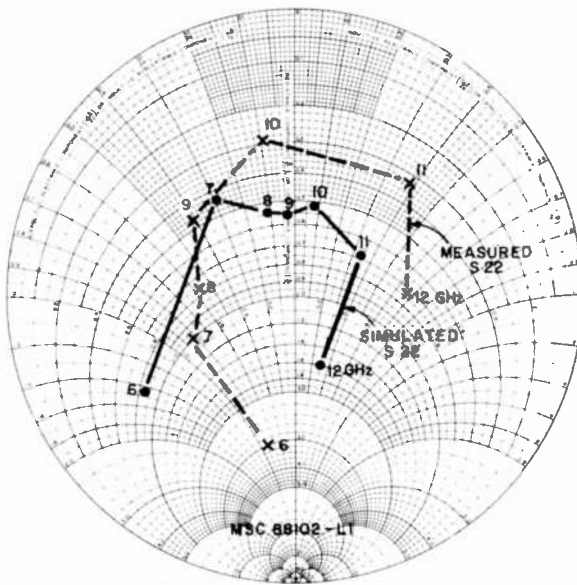

Fig. 9—Simulated and measured matched carrier S_{22} coefficient for MSC 88102.

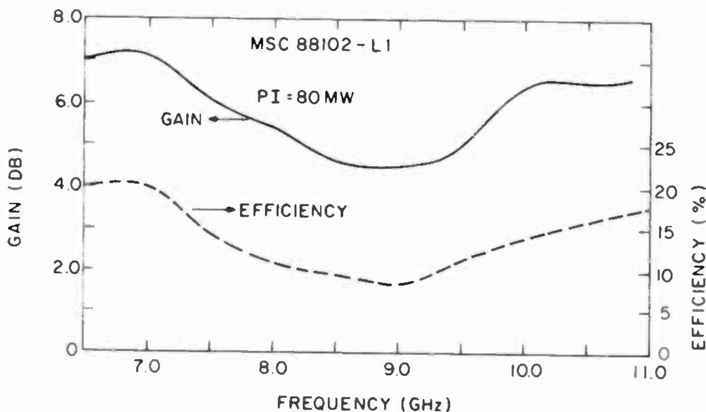

Fig. 10—Gain and power-added efficiency versus frequency for MSC 88102.

end of the band and 20% at the low end, with a minimum of 8.5%. The minimum efficiency can definitely be improved with a better input matching network.

The efficiency of an amplifier can also be dramatically improved with a more stringent device selection process. This is illustrated by observing the performance variations for a number of amplifiers assembled from within the same batch of purchased transistors. Fig. 11 is a plot of the gain versus frequency for four (E2, E4, E7, E10) lumped-element,

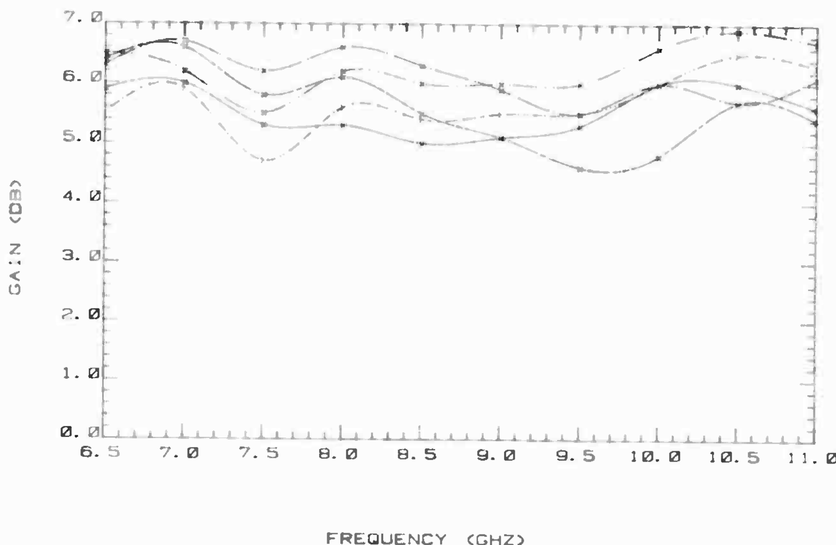

Fig. 11—Gain versus frequency for four (E2, E4, E7, and E10) lumped-element matched MSC 88102 devices (P_I = 80 mW, V_G = 2 V, and V_D = +8 V).

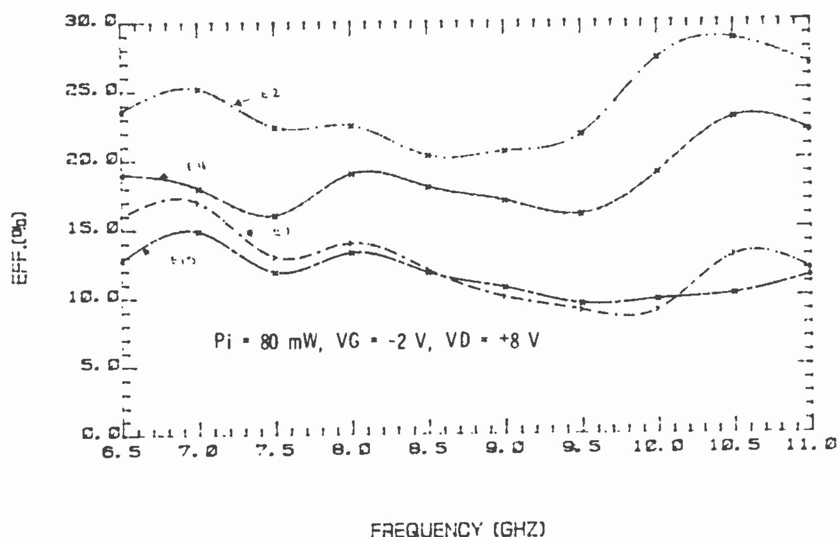

Fig. 12—Efficiency versus frequency for four lumped-element matched MSC 88102 devices.

matched transistors measured under the same operating conditions. For 80 mW of input power, these amplifiers typically have an output power in excess of 300 mW across the band from 6.5–11 GHz. Fig. 12 summarizes the efficiency versus frequency for the same four matched carriers. The efficiency variation within this small sample of devices is very great, with the best device showing that 28% efficiency is possible. Even in this best result though, the same performance degradation in the center portion of the band is evident. The large efficiency variation is due to the device operating-current fluctuations. This variation can be decreased but not eliminated by a dc parameter selection process. Some statistical information about how the dc selection could be performed is presently being formulated.

4.2 2400-μm Gate-Width Design

Using the same lumped-element circuit topology with slightly different element values, a 2400-μm width service was matched from 6–12 GHz. A photograph of the MSC 88104 matched device is shown in Fig. 13 with capacitor elements and values identified. The output shunt capacitor for this circuit is slightly larger (0.45 pF) than in the 1200-μm MSC 88102 case. A scale is included in the photograph so that inductor lengths may be directly estimated. The total matched carrier is 1.6 × 2.4 mm.

The design approach and the resulting performance qualitatively agree

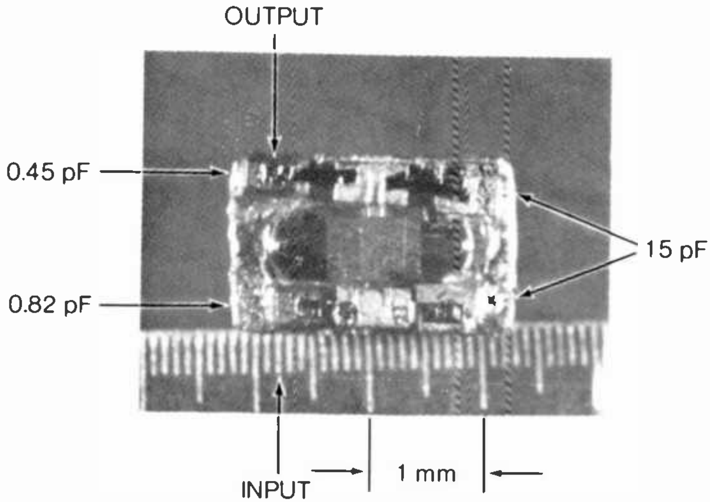

Fig. 13—6–12 GHz matched carrier showing element values.

with the results previously presented for the smaller gate-width design. The problems associated with the high input reflection coefficient are more pronounced and much more difficult to deal with. This is illustrated by the series of reflection coefficient plots in Figs. 14, 15, and 16. In Fig. 14, the input and output mismatch gain is ploted versus frequency. The mismatch gain is defined as the magnitude of gain that may be realized if the input (G_1) or output (G_2) is perfectly matched. For both the input and the output, very little additional gain can be achieved at the high

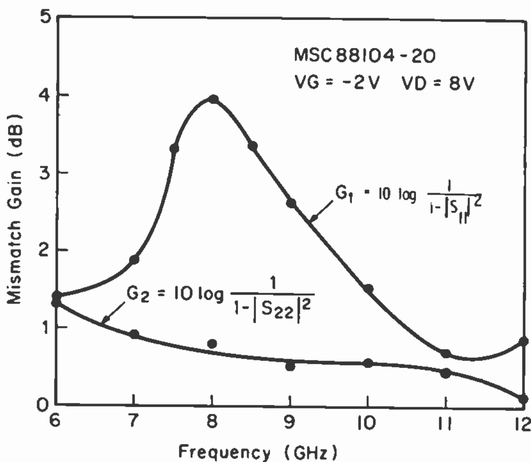

Fig. 14—Input (G_1) and output (G_2) gain equalization for MSC-88104 from 6–12 GHz.

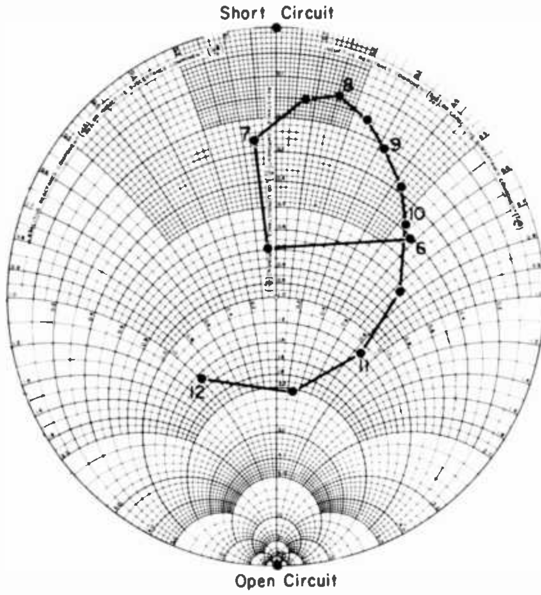

Fig. 15—Measured S_{11} coefficient plot for MSC 88104.

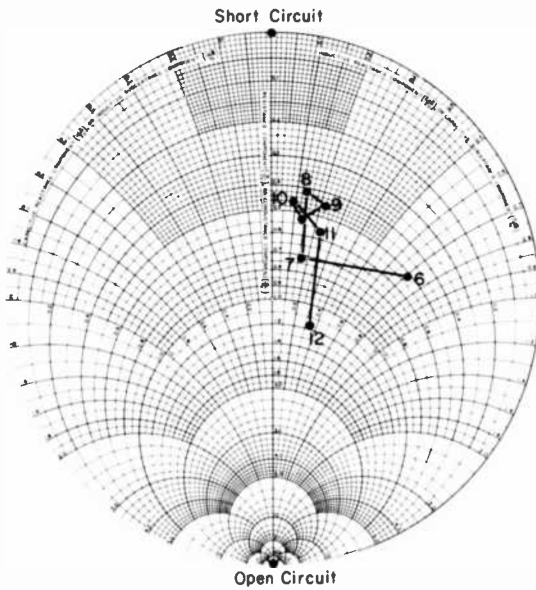

Fig. 16—Measured S_{22} coefficient for MSC 88104.

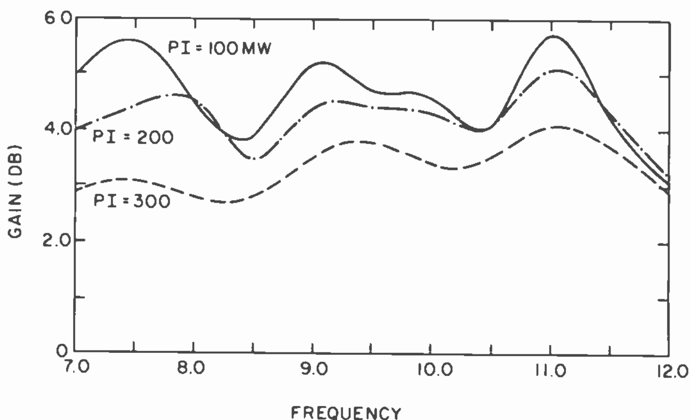

Fig. 17—Gain versus frequency for a lumped-element matched MSC 88104 ($V_G = -2$ V, $V_D = 9$ V, $I_D = 400$ mA).

end of the frequency band. As frequency decreases, gain is selectively sacrificed by reactively mismatching the device. This is a classical gain equalization approach that flattens the overall amplifier gain by controlling the input and output mismatch gain slopes. In the 2400-μm width MSC 88101 design, the slope and magnitude of the input mismatch gain is larger than desired. The output match in this design is not a problem, although some additional experiments to purposely mismatch the output to achieve more power are underway. Fig. 15 and 16 are input (S_{11}) and output (S_{22}) reflection coefficient plots for the same device and are included for completeness.

The gain and output power performance for the MSC 88104-20

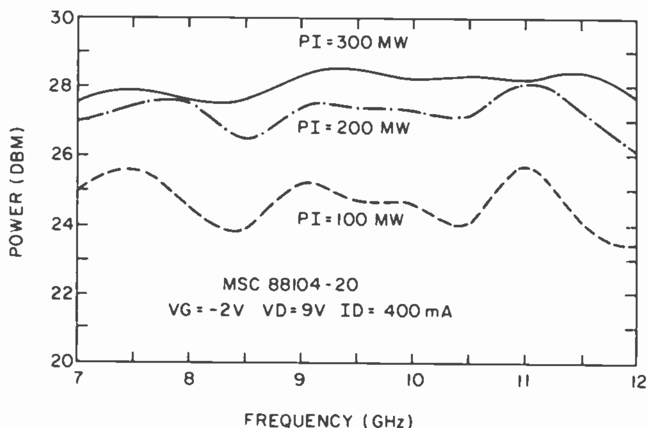

Fig. 18—Output power versus frequency for lumped-element matched MSC 88104.

matched carrier are summarized in Fig. 17 and 18. These plots show that this device is capable of achieving output power in excess of 0.5 W at a gain of greater than 4 dB. The efficiency of this matched carrier is nominally 10% at the 0.5-W output power level.

A very brief comparison between the two matched carrier designs and the results obtained is in order at this point. First, it seems that higher efficiency is attainable with the 1200-μm width MSC 88102 device in a broadband amplifier covering the 6–12 GHz frequency range. Repeatable efficiencies in the 20% range are achievable for this device, whereas 10% is more typical in the larger 2400-μm width MSC 88104 design. Also, for twice the gate width, the output power does not double as, theoretically, it should. However, to achieve more than 0.5 W per transistor broadband, it is necessary to use the larger 2400-μm width device.

5. Broadband Amplifier Performance

In this section, we show how lumped-element matched combiners can be integrated into stand-alone amplifier stages including bias injection mechanisms. In addition, two examples of broadband multi-stage amplifiers are given—a 6–11 GHz, 1-W, two-stage amplifier and a 7–12 GHz, 1-W, four-stage amplifier. Since all rf matching is performed in a lumped-element format, conventional microstrip-transmission-line techniques using quartz substrates are used to cascade and combine matched carriers. Quartz substrates are used because of their low-loss J-band properties and also because repeatable interdigitated combiners have been fabricated using this material.

5.1 Lumped-Element Power Amplifier Stage

Fig. 19 is a photograph of a lumped-element power stage pallet including the rf matched GaAs FET carrier, bias circuitry, and associated printed transmission lines. The complete amplifier pallet, which carries all components, is made of kovar and measures 1.27 × 1.59 cm. The quartz substrates, supplied by Accumet, Inc., are 0.38 mm thick and are metallized by us using cermet/copper/gold. The bias networks consist of Alpha beam lead dc blocking capacitors in series with the 50Ω interconnecting lines. On the gate side of the device, bias is injected through a high value resistor (200 Ω), the value of which is noncritical. This resistor provides a means for injecting a gate voltage, while at the same time providing an open circuit to the rf path. It is possible to use a resistor in the gate circuit since only leakage current flows through the device Schottky barrier. On the drain side of the device, a quarter-wave high-impedance line is used that is shorted at one end by a parallel-plate ca-

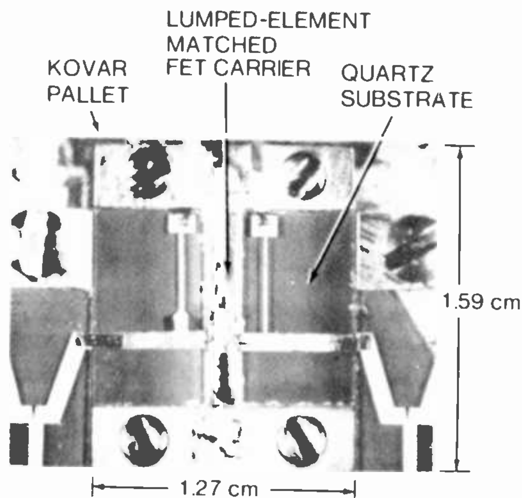

Fig. 19—6–11 GHz MSC 88102 power amplifier stage.

pacitor. In this current, the short is transformed into an open circuit by the high impedance (narrow) printed line. A resistor on the drain side of the device is not possible, because high currents are drawn.

The performance of a single-stage amplifier with bias circuitry is similar to that of a matched carrier alone. The bias lines do tend to degrade the high end of the band slightly, which has been traced to the parasitic inductance at the edge of the substrate where the high im-

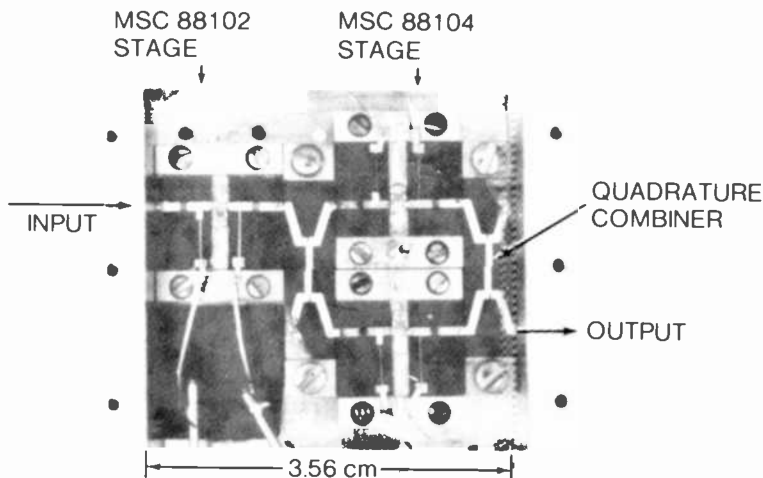

Fig. 20—6–11 GHz, 1-W, two-stage amplifier.

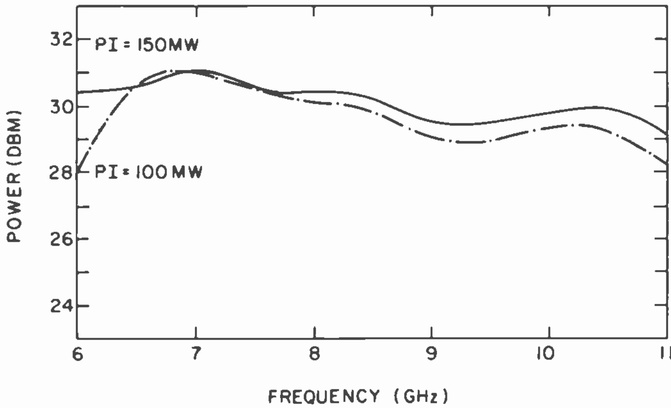

Fig. 21—6–11 GHz two-stage amplifier output power versus frequency (V_D = 10 V).

pedance line is shorted by the parallel-plate capacitor. Various methods for eliminating bias circuit effects are being investigated for the drain side of the device.

5.2 6–11 GHz, 1-W, Two-Stage Amplifier

Once the kovar amplifier pallets have been assembled and tested, they may be combined or cascaded into any configuration desired. Fig. 20 illustrates a two-stage, 1-W, 6–11 GHz amplifier in which two MSC 88104

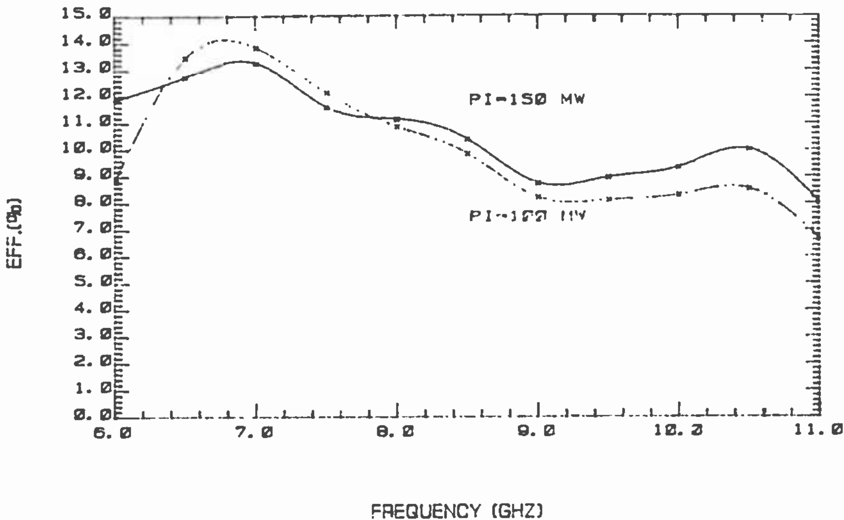

Fig. 22—6–11 GHz two-stage amplifier power-added efficiency versus frequency.

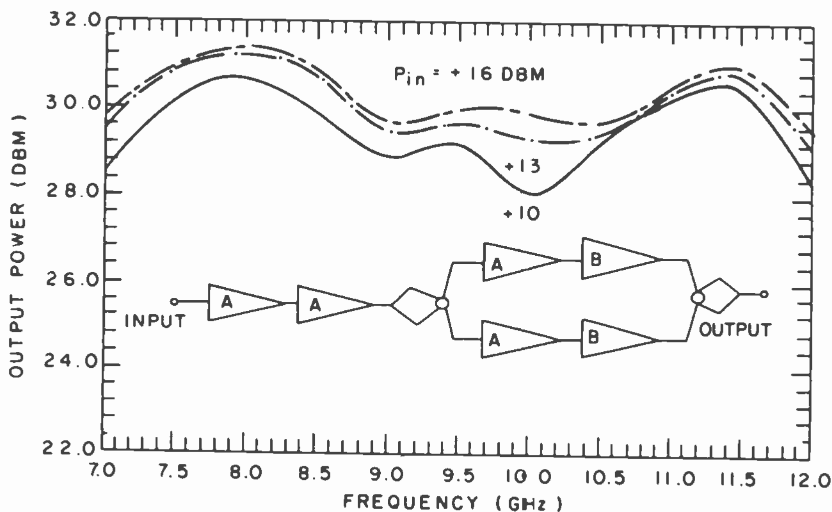

Fig. 23—Output power versus frequency for a 7–12 GHz, 1-W saturated four-stage amplifier.

amplifier stages are combined using interdigitated combiners in a balanced amplifier configuration. The balanced stage is then driven by a stage that uses an MSC 88102 matched device. The output power, efficiency, and performance for the amplifier is summarized in Figs. 21 and 22. This amplifier has a nominal saturated output power of 1 W and power-added efficiency of 10% across the 6–11 GHz frequency band for an input power of 150 mW.

5.3 7–12 GHz, 1-W, Four-Stage Amplifier

Fig. 23 summarizes the performance of a 7–12 GHz, 1-W, four-stage amplifier. The amplifier consists of three, two-stage, lumped-element amplifier modules, two of which are combined at the output with an in-phase combiner. In each amplifier module, all rf matching is achieved in a lumped-element format. The matched devices are directly cascaded with short, 50 Ω microstrip transmission lines. The output amplifier modules are 1.25 cm square; the input driver was made slightly larger for convenience in assembly. The overall amplifier bandwidth is mainly determined by the passive combiners.

6. Conclusion

A unique broadband circuit has been developed that allows individual elements within the topology to be optimized using a special fixture.

Using this circuit, very small lumped-element matched amplifiers have been developed that cover the 6–12 GHz bandwidth with 0.3-W and 0.6-W minimum output power levels. Using these matched carriers, a 1-W, 7–12 GHz, multi-stage amplifier has been developed.

Broader bandwidth and higher power extensions of this work are possible and are currently in progress. Broader bandwidth is possible if the device and its package are more favorably utilized; higher powers are possible by combining devices on the chip level and by using passive combiners.

Acknowledgments

The authors wish to acknowledge the technical support of W. Cvecich in the fabrication and testing of the interdigitized quartz combiners. We also acknowledge the encouragement and support of this work by S. Y. Narayan and F. Sterzer.

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Fabrication of Lumped-Element Broadband GaAs MESFET Microwave Power Amplifiers

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Abstract—Methods have been developed to automate the fabrication of lumped-element GaAs MESFET power amplifiers. Lumped-element circuit components are used in an on-carrier construction that allows fabrication of small-size amplifiers. The amplifier stages are designed for wideband (6–11 GHz) operation with a minimum power output of 27.8 dBm and 3-dB gain. Component value sensitivity studies showed a narrow value range that is counterpoised by prudent use of bond-wire inductance. Areas discussed include device-to-device variations and associated statistical data, evaluation of bond-wire inductance and measurements, capacitor selection criteria, optimization of performance under computer control, and circuit design techniques. Emphasis is on performance trimming and automated assembly.

1. Introduction

This paper describes techniques developed for automated fabrication of wideband, lumped-element matched, GaAs MESFET amplifiers. Ongoing research at RCA Laboratories has shown that wideband (6–11 GHz) operation, significant size reduction, and circuit simplicity can be achieved using lumped-element matching techniques for these amplifiers.[1] The state-of-the-art has now reached a stage where fabrication of lumped-element amplifiers can be carried out using automated as-

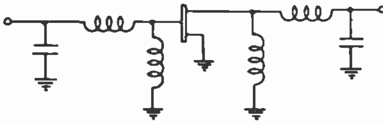

Fig. 1—Circuit diagram of power amplifier stage.

sembly equipment on a majority of the operations by personnel without the special skills of a design group.

A single-stage power amplifier using the MSC 88104 GaAs MESFET* was chosen as the test vehicle. The design goals were:

Frequency range: 6–11 GHz	Power gain: 3 dB (minimum)
Output power: 27.8 dBm (minimum)	Efficiency: 10% (minimum)

Fig. 1 shows the circuit diagram of the power amplifier stage. The inductor elements are realized using 25.4 μm (0.001 inch) gold bond wires. The capacitor elements are commercially available thin-film capacitors. The objective is to realize the proper inductances using an automatic wire bonder. To develop a systematic procedure for fabricating these amplifiers the following tasks were carried out.

(1) A sample of 30 MSC 88104 GaAs MESFETs were purchased. The S-parameters of these FETs were measured using an automatic network analyzer to obtain statistical data on device-to-device variations. Based on this data, a standard MESFET equivalent circuit was generated for use in the circuit design.
(2) Following circuit design, a sensitivity analysis was performed with each component value varied around the design parameter. The allowable "windows" for each component were determined.
(3) A test fixture was developed for evaluating bond-wire inductance. This fixture closely matches the amplifier configuration. Design curves for estimating and predicting bond-wire inductances were generated.
(4) Capacitors from several manufacturers were evaluated. Small size and low dissipation factors were the selection criteria.
(5) A computer program (ZIMP) was developed to allow amplifier optimization at the point of manufacture. This allows changes in bond-wire inductance and capacitor values to be made to bring the amplifier performance into close agreement with the design.

* Microwave Semiconductor Corp., Somerset, NJ 08873.

Table 1—Performance Data of Lumped Element FET Amplifiers

Amplifier No.	Gain (dB) (24.8 dBm Input)	Output Power (mW) @ 11 GHz	Efficiency (%)
A-4	3.14	618	15.3
A-6	3.36	651	18
A-9	3.03	602	13
A-10			
A-11	3.09	611	12.1
A-13	3.74	710	18.5
A-14	3.0	600	12
A-16	2.8	562	16
A-17	3.73	709	19.1
A-18	3.25	620	17
A-19	4.26	800	19
A-20	2.7	555	12
A-27	4.45	836	17
A-33	3.2	623	13.4
A-34	3.0	600	17.3
A-40	4.0	751	13
A-21	2.43	525	12.7
A-24	3.0	600	16.5

After developing these techniques the amplifiers were fabricated at RCA Automated Systems and evaluated at RCA Laboratories. Table 1 shows the performance of the amplifiers at 11 GHz, the band-edge frequency. Fig. 2 shows the performance of the amplifier over 6–11 GHz. Figure 3 is a photograph of the lumped element amplifier stage.

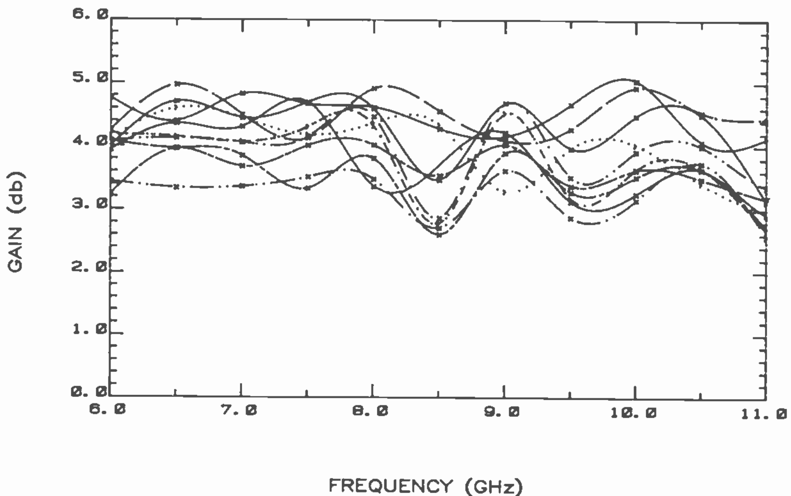

Fig. 2—Multiplot of power performance.

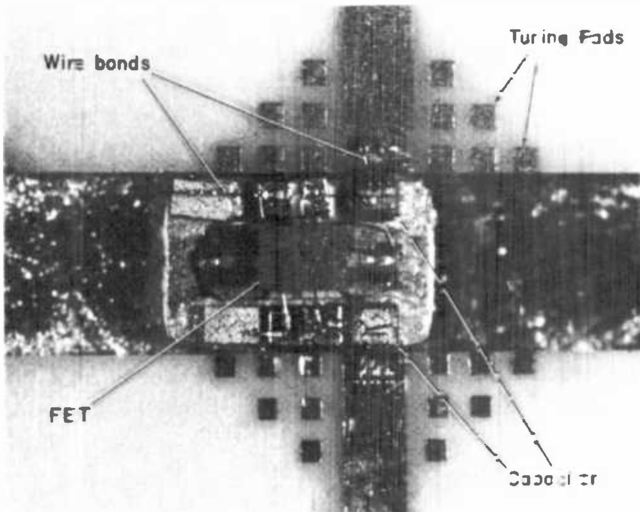

Fig. 3—Lumped-element amplifier.

2. MSC 88104 GaAs MESFET

The MSC 88104 (2400 μm gate width) device is the design vehicle. This transistor comes in a package that offers a substantial area in which to

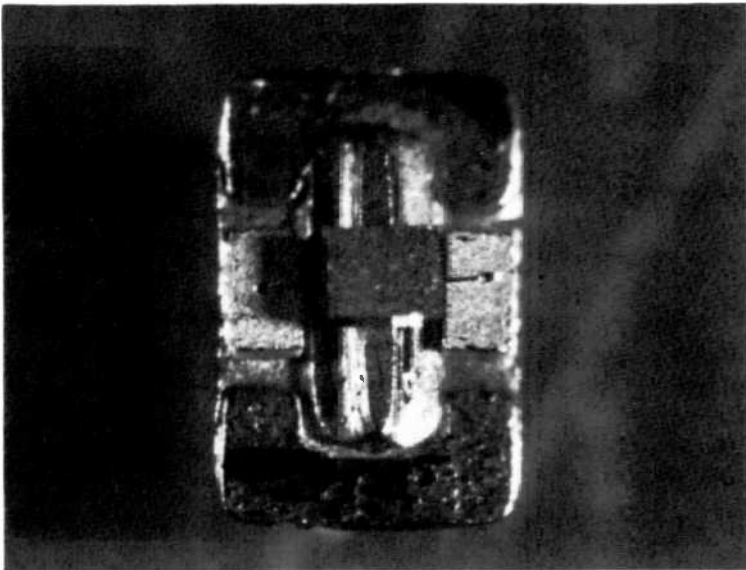

Fig. 4—FET package.

attach lumped-element components. One can construct the complete matching network for both the gate and drain elements within the package area. Shown in Fig. 4 is the package with the FET flip-chip mounted to the pedestal located at center. Flying wires to standoffs provide the connection to the gate and drain elements. The areas to the right and left of the standoffs are used for mounting lumped elements.

Each GaAs MESFET received for this program was subjected to dc and rf characterization. DC tests were made on a curve tracer and rf testing was performed on an automatic network analyzer. To reduce heat cycling and possible damage due to multiple soldering operations, a quick connecting test fixture was used. The fixture allows rf testing without solder mounting the device on a carrier. The dc specifications of the MSC 88104 are:

I_{DSS} = 500 to 900 mA at 5 V

G_m = 140 m℧

Reverse $V_{25} = -8$V at 160 μA

The rf specifications are:

Output power = 29 to 30 dBm at 12 GHz

Gain at 1 dB compression = 5 dB at 12 GHz

A total of 20 FET amplifiers were constructed. All the transistors used were obtained as part of a single order and small-signal S-parameter data was obtained for each device. This S-parameter data was then tabulated and ordered to yield statistical information which defines a "standard" FET on which to base the amplifier design. These data, given in Table 2, are discussed in Sec. 9.

Table 2—Standard FET S-Parameter Data Based on 20 Devices

FREQ	S11		S21		S12		S22	
6.0	.840	−176.6	1.308	40.5	.067	−11.4	.466	−155.5
7.0	.860	172.4	1.083	30.3	.060	−13.3	.523	−180.8
8.0	.861	172.9	.925	19.9	.055	−9.6	.580	−159.8
9.0	.860	170.5	.820	12.1	.055	−9.4	.627	−162.8
10.0	.857	166.3	.732	4.5	.051	−12.3	.656	−164.4
11.0	.863	159.2	.641	−4.6	.046	−11.9	.673	−165.6
12.0	.866	154.6	.561	−9.7	.043	−10.0	.693	−167.0

3. Amplifier Power Stage

Using the S-parameters of the "standard" MSC 88104 GaAs FET, we develop the matching topologies needed to transform the very low device

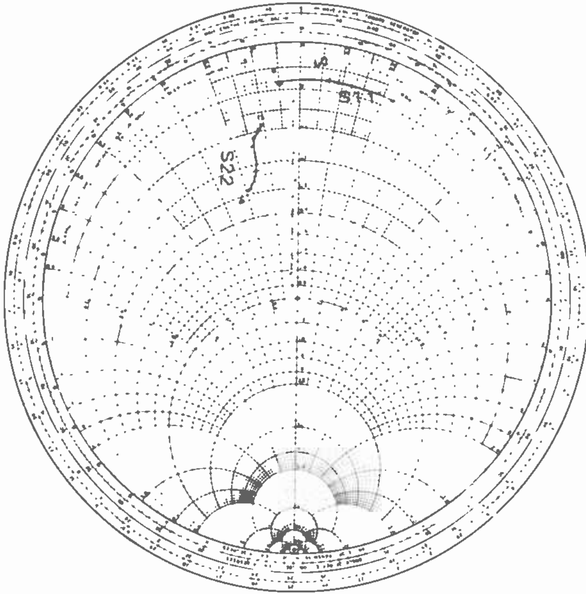

Fig. 5—Reflection coefficient plot of "standard" FET.

impedances to the 50 Ω system. Since any circuit containing inductors and capacitors is frequency-dependent and device performance is gain deficient at 11 GHz, the design was optimized at this frequency. Essentially, we are looking at a single frequency and, therefore, the matching networks need not be complicated. From the standard FET S-parameter data shown in Fig. 5, a matching circuit must be determined that will best fit the amplifier goals in terms of practicability of realization and ease in biasing. From the S_{11} term at 11 GHz, it can be seen that a circuit consisting of a series L and shunt C or a series C and shunt L will both perform the necessary transformation to the 50 Ω system.

The low-pass circuit configuration was chosen because it allows us the option to trim performance using only the inductors. The capacitors are fixed in value before assembly. Since the inductor will be the only component varied, we needed to know how small wire inductors behave in our carrier topology. The inductor measurements are described in Sec. 5.

The preferred design is based on the standard data derived from the S-parameter measurements and is adjusted for each device during assembly. In this manner, each amplifier will be partially optimized before rf testing begins.

The series inductor values are determined by taking the difference between the measured reactance and the reactance at the intersection

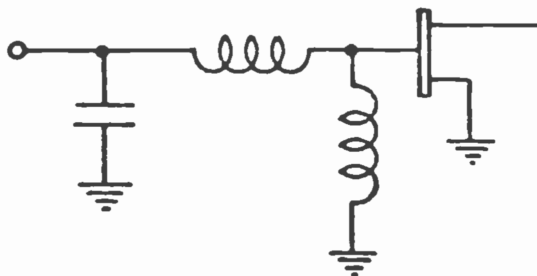

Fig. 6—Input circuit.

of the constant conductance circle on the Smith Chart. The shunt element value is obtained from the capacitive reactance at this point. In terms of S-parameters,

$$\frac{Z_{(\omega)}}{Z_0} = \frac{1 + S_{(\omega)}}{1 - S_{(\omega)}}$$

where $S = S_{11}$ or S_{22} and $Z_{(\omega)} = r + jx$, and

$$Y_{(\omega)} = \frac{1}{Z_{(\omega)}},\ Y_{(\omega)} = G + jB$$

$$L = \frac{x}{\omega} Z_0$$

$$C = \frac{B}{\omega} Y_0$$

Observing the spread in the phase of the coefficients of the S_{11} term across the 6–11 GHz frequency band, we note that at 6 GHz, a shunt L will contribute to the overall match without appreciably affecting the frequencies at the high end. The input circuit is now defined and is shown in Fig. 6. The output circuit is designed in a similar manner emphasizing fabrication simplicity and bias.

In broadband microwave designs, tradeoffs must be made in gain at the lower frequencies for maximum gain at the high end. Basically, this selective mismatching is achieved by tailoring the gain contribution of both the input and output circuits. The mismatch gain is determined by

$$\text{Gain} = 10 \log \frac{1}{1 - |S|^2}$$

and compensates for transducer gain therefore yielding a constant gain across the band of interest. As shown in Table 3, the design works best

Table 3—Reflection Coefficients of Completed Circuit

S --MAGN AND ANGLES:

FREQ	11		21		12		22	
6000.0	.535	-157	2.476	75	.094	9	.392	152
6500.0	.639	-173	2.194	53	.088	-8	.323	150
7000.0	.679	171	1.997	35	.085	-25	.277	148
7500.0	.739	159	1.974	19	.087	-41	.246	153
8000.0	.754	143	1.935	-3	.091	-62	.208	148
8500.0	.754	130	1.892	-21	.096	-77	.187	147
9000.0	.721	116	1.859	-38	.101	-92	.144	141
9500.0	.654	101	1.852	-56	.110	-108	.127	126
10000.0	.568	84	1.920	-76	.123	-125	.086	105
10500.0	.433	55	1.973	-99	.133	-145	.099	43
11000.0	.342	6	1.949	-125	.142	-168	.148	-8
11500.0	.436	-51	1.835	-155	.143	164	.298	-48
12000.0	.604	-94	1.451	173	.124	136	.398	-80

FREQ	H21	S21	G1	G2	GMAX	U	K
6000.0	12.7	7.9	1.5	.7	10.1	.03	1.41
6500.0	10.1	6.8	2.3	.5	9.6	.07	1.40
7000.0	8.7	6.0	2.7	.3	9.0	.06	1.43
7500.0	8.3	5.9	3.4	.3	9.6	.07	1.16
8000.0	8.3	5.7	3.6	.2	9.6	.07	1.11
8500.0	8.7	5.5	3.6	.2	9.3	.06	1.11
9000.0	9.4	5.4	3.2	.1	8.7	.04	1.25
9500.0	10.9	5.4	2.4	.1	7.8	.03	1.42
10000.0	13.2	5.7	1.7	.0	7.4	.02	1.50
10500.0	14.6	5.9	.9	.0	6.8	.01	1.63
11000.0	12.3	5.8	.5	.1	6.4	.02	1.68
11500.0	9.4	5.3	.9	.4	6.6	.04	1.59
12000.0	5.9	3.2	2.0	.7	6.0	.08	1.72

at the high and low ends of the frequency band but the gain is slightly suppressed at the band center. Figure 7 depicts the power-gain performance of the best and worst case amplifiers. The different gains are due to the difference in device current. Where device A40 had an I_{DSS} of 850 mA, device A16 had only 600 mA I_{DSS}. The important considerations are a minimum acceptable gain of 3 dB below which the amplifier must be optimized.

4. Circuit Simulation

Synthesis of the circuit can be made by modeling the known component values into a computer program such as compact.* The program will print out the predicted performance that should be realized when the circuit is constructed.

* Compact Engineering, 1131 San Antonio Rd., Palo, Alto, CA 94303.

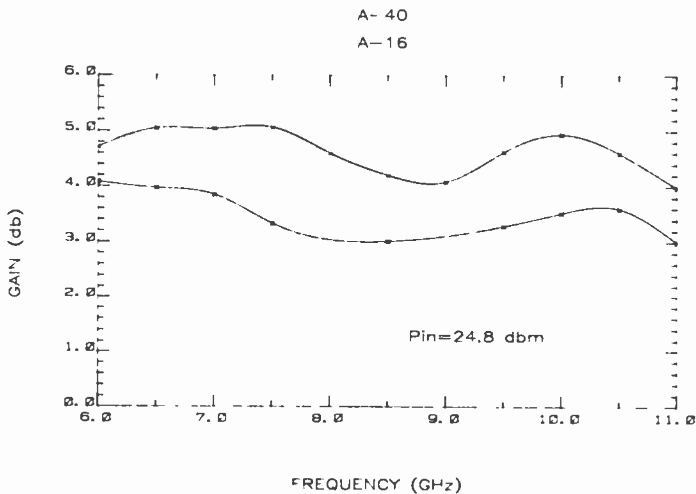

Fig. 7—Power-gain performance of best and worst case amplifiers.

A sensitivity analysis was performed with each component varied around its design value and gain prediction. As can be seen in Tables 4a and 4b, a significant gain increase can be realized by increasing the value of the input capacitor by 0.1 pF. However, there is a gain reduction at 11 GHz. An overall gain change occurs by decreasing this value 0.1 pF below the design value, as shown in Table 4c. The sensitivity of the output capacitor is depicted in Tables 4d and 4e. The same trend is evident in the output capacitor except that the value takes on more importance at the operating power level. The tight allowable range into which both capacitors must fall for proper circuit performance is seen from this data. The capacitor value used in the actual circuit must be measured before assembly, since changing these components is not practical.

In Table 5a the value of the series inductor on the input circuit was reduced by 0.05 nH with the effect of an overall gain decrease. Increasing the value 0.1 nH above the design value yields a 1-dB increase in gain over most of the band but not at 11 GHz, where it is needed most (Table 5b).

The value of the series inductor on the output circuit is less sensitive as shown in Tables 5c and 5d. Here the inductor was varied ±0.1 nH from the design value with only a 0.5 dB decrease in gain. It should be clear that the output circuit will become a factor when the circuit is operated at the required power levels where optimum matching of the load impedance is required.

Table 4

a. Computer simulation of circuit with design values.

FREQ	S11		S21		S12		S22		GAIN	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	DB	DEG
6000.0	.874	170.4	1.774	42.34	.080	-10.9	.218	120.8	4.978	42.34
7000.0	.875	164.3	1.634	14.65	.081	-29.3	.176	152.9	4.266	14.65
8000.0	.816	154.7	1.657	-12.4	.088	-39.6	.284	-174.	4.337	-12.4
9000.0	.706	145.1	1.680	-38.0	.102	-57.9	.332	175.1	4.506	-38.0
10000.	.500	118.0	1.808	-72.1	.117	-89.1	.247	150.2	5.145	-72.1
11000.	.337	5.613	1.867	-124.	.121	-132.	.070	60.84	5.423	-124.

b. Input capacitor value increased .1 pf.

FREQ	S11		S21		S12		S22		GAIN	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	DB	DEG
6000.0	.870	170.3	1.798	41.58	.081	-11.6	.205	120.8	5.097	41.58
7000.0	.868	163.9	1.678	13.63	.083	-30.3	.174	157.6	4.495	13.63
8000.0	.797	153.6	1.732	-14.3	.092	-41.5	.301	-172.	4.770	-14.3
9000.0	.661	143.0	1.773	-41.6	.103	-61.5	.358	174.8	4.999	-41.6
10000.	.385	109.8	1.927	-79.5	.125	-96.5	.271	144.5	5.697	-79.5
11000.	.336	-43.2	1.829	-137.	.118	-145.	.095	40.57	5.244	-137.

c. Input capacitor value decreased .1 pf.

FREQ	S11		S21		S12		S22		GAIN	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	DB	DEG
6000.0	.878	170.5	1.750	43.08	.079	-10.1	.231	120.8	4.859	43.08
7000.0	.882	164.6	1.592	15.61	.079	-28.3	.180	148.4	4.041	15.61
8000.0	.833	155.8	1.587	-10.5	.084	-37.8	.270	-176.	4.011	-10.5
9000.0	.743	147.1	1.587	-34.8	.097	-54.7	.309	175.0	4.010	-34.8
10000.	.593	124.8	1.680	-65.7	.109	-82.7	.222	154.7	4.509	-65.7
11000.	.409	51.57	1.809	-111.	.117	-119.	.044	89.31	5.150	-111.

d. Output capacitor value increased .1 pf.

FREQ	S11		S21		S12		S22		GAIN	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	DB	DEG
6000.0	.862	171.1	1.822	36.68	.082	-16.5	.129	129.0	5.211	36.68
7000.0	.870	164.9	1.683	8.319	.083	-35.6	.156	-176.	4.521	8.319
8000.0	.808	154.8	1.716	-19.3	.091	-46.6	.327	-162.	4.693	-19.3
9000.0	.687	143.7	1.779	-46.8	.103	-66.7	.357	-176.	5.003	-46.8
10000.	.420	107.8	1.960	-86.6	.127	-104.	.203	162.7	5.847	-86.6
11000.	.421	-41.4	1.817	-147.	.117	-156.	.143	-66.7	5.188	-147.

e. Output capacitor value decreased .1 pf.

FREQ	S11		S21		S12		S22		GAIN	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	DB	DEG
6000.0	.880	169.7	1.763	46.33	.079	-5.87	.262	119.7	4.925	46.33
7000.0	.870	162.9	1.659	18.87	.082	-25.0	.228	141.7	4.395	18.87
8000.0	.789	152.3	1.734	-9.26	.092	-36.6	.297	171.9	4.781	-9.26
9000.0	.638	141.8	1.763	-36.4	.107	-56.3	.379	166.3	4.924	-36.4
10000.	.348	110.8	1.867	-72.6	.121	-89.6	.361	138.1	5.423	-72.6
11000.	.360	-47.0	1.780	-126.	.115	-135.	.243	82.40	5.005	-126.

The averages of the computer simulation of gain variation with component value change over the frequency band is listed in Table 6.

5. Wire Inductance

The inductance of a very short length of wire is extremely difficult to

Table 5

a. Series input inductor decreased .05 nh.

FREQ	S11		S21		S12		S22		GAIN	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	DB	DEG
6000.0	.883	173.6	1.711	44.06	.077	-9.14	.222	119.4	4.666	44.06
7000.0	.889	162.8	1.550	17.09	.077	-26.8	.171	150.7	3.808	17.09
8000.0	.843	161.5	1.543	-8.60	.083	-35.9	.272	-173.	3.765	-8.60
9000.0	.761	155.1	1.537	-32.3	.094	-52.2	.317	177.4	3.735	-32.3
10000.	.615	137.7	1.645	-62.4	.107	-79.4	.238	157.6	4.326	-62.4
11000.	.348	71.78	1.857	-107.	.120	-116.	.067	103.2	5.385	-107.

b. Series input inductor increased .1 nh.

FREQ	S11		S21		S12		S22		GAIN	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	DB	DEG
6000.0	.847	161.8	1.931	37.80	.037	-15.4	.212	124.6	5.716	37.80
7000.0	.837	151.3	1.852	7.835	.092	-36.1	.193	157.3	5.355	7.835
8000.0	.732	133.2	1.954	-23.5	.104	-50.8	.318	-177.	5.818	-23.5
9000.0	.529	108.2	2.012	-55.5	.123	-75.4	.365	166.7	6.074	-55.5
10000.	.322	21.87	1.976	-100.	.128	-117.	.234	128.4	5.916	-100.
11000.	.675	-72.1	1.464	-155.	.095	-164.	.090	-7.51	3.309	-155.

c. Series output inductor decreased .1 nh.

FREQ	S11		S21		S12		S22		GAIN	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	DB	DEG
6000.0	.883	170.9	1.785	36.52	.080	-16.7	.183	87.34	5.034	36.52
7000.0	.871	164.4	1.656	7.395	.082	-36.5	.074	107.5	4.379	7.395
8000.0	.840	154.4	1.709	-20.8	.091	-49.1	.149	-169.	4.656	-20.8
9000.0	.735	143.0	1.764	-49.5	.108	-69.4	.140	170.8	4.929	-49.5
10000.	.512	111.0	1.862	-88.9	.121	-106.	.065	5.251	5.400	-88.9
11000.	.377	-5.02	1.745	-145.	.113	-154.	.362	-49.1	4.834	-145.

d. Series output inductor increased .1 nh.

FREQ	S11		S21		S12		S22		GAIN	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	DB	DEG
6000.0	.867	159.8	1.745	48.03	.078	-5.17	.280	144.2	4.836	48.03
7000.0	.861	163.9	1.589	21.62	.079	-22.3	.289	169.5	4.023	21.62
8000.0	.793	154.6	1.577	-4.58	.084	-31.9	.409	-171.	3.958	-4.58
9000.0	.673	146.2	1.551	-27.9	.095	-47.8	.492	-177.	3.812	-27.9
10000.	.466	123.2	1.634	-57.4	.106	-74.4	.483	170.2	4.265	-57.4
11000.	.267	11.68	1.732	-102.	.112	-111.	.379	153.6	4.772	-102.

measure, it is also greatly influenced by its environment. It is best measured in a fixture that matches, as closely as possible, the geometry of the actual amplifier in order to account for the high stray parasitic inductance and capacitances. A test fixture connected to a bypass capacitor that is the same as that used in the circuit was constructed utilizing a 50 Ω microstrip line of the same length as that used on the actual amplifier carrier and terminated by the inductor under test. By knowing the transmission-line wavelength and measuring at the $\lambda/2$ frequency, parasitic effects can be minimized.

Since the structure is very much like the amplifier, the inductance values should be near the actual inductor with its parasitics. It is very

Table 6—Computer Simulation of Gain Variation

	Deviation from Design Value	Average Gain Change (dB)
Input Capacitor	+0.1 pF −0.1 pF	+0.26 −0.35
Output Capacitor	+0.1 pF −0.1 pF	+0.3 +0.13
Input Inductor	+0.1 nH −0.05 nH	+0.6 −0.5
Output Inductor	+0.1 nH −0.1 nH	−0.5 +0.1

important that the calibration of the test system be as accurate as possible, since small changes in the length of the reference will cause significant errors in the inductance measurement. Secondly, very accurate frequency stability and reproducibility must be maintained if observations are to be made on inductor length changes. For these reasons all measurements were performed on a phase-locked automatic network analyzer.

For very short wire lengths, the self-inductance at microwave frequencies is[3]

$$L = 5.08\, l\left(\ln \frac{4l}{d} - 1 + \frac{d}{2l}\right)$$

where L is the inductance in nH, d the wire diameter in inches and l the

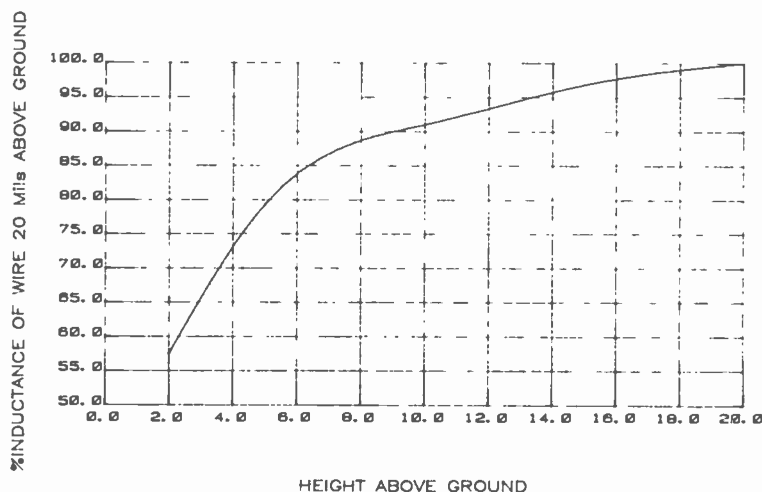

Fig. 8—Inductance versus height above ground (1 mil dia. wire).

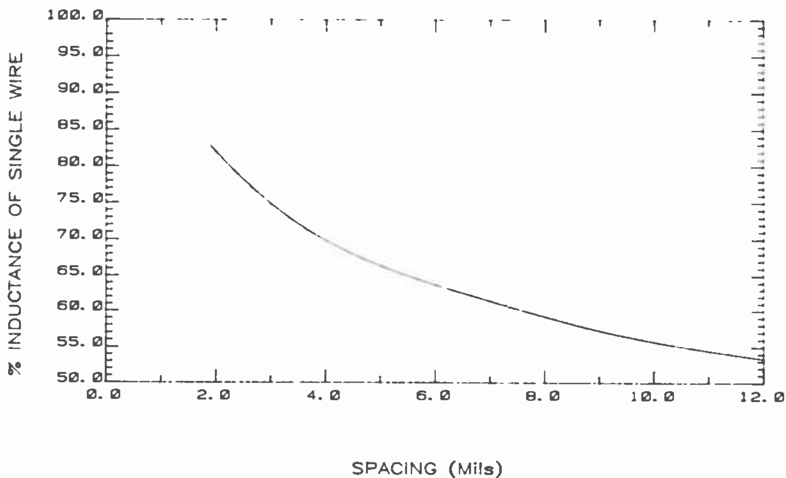

Fig. 9—Parallel wire inductance and spacing (1 mil dia. wire).

length of the wire. The value of inductance is reduced when the spacing between the parallel ground plane and inductor is small. Fig. 8 is a plot of the effective inductance versus distance from ground. The effect could be used to trim performance of the amplifier if it were not for the increase in losses due to higher currents. A more acceptable method of trimming amplifier performance when the inductor value is too large would be to parallel the wires. Due to the tight spacing requirements set by the small

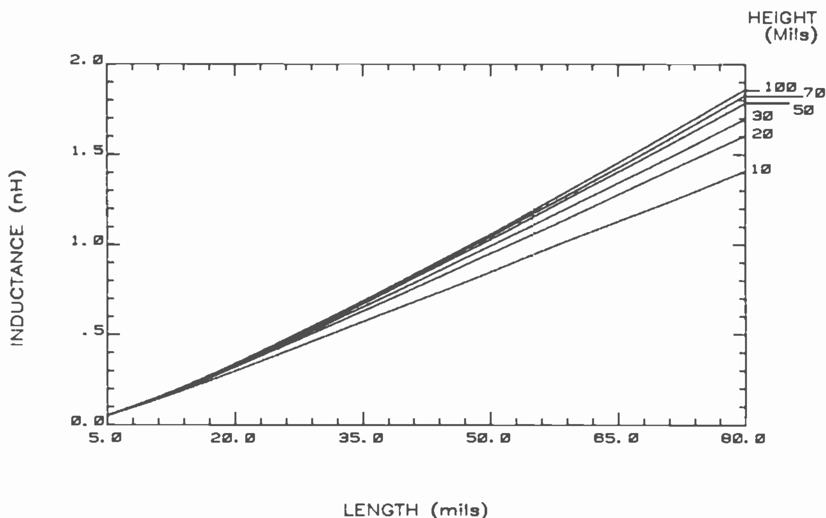

Fig. 10—Inductance versus wire length (1 mil dia. wire).

component size, the effective inductance decreases as a function of the spacing between wires. The effect is caused by the mutual inductance between the adjacent wires. Fig. 9 gives the measured inductance change as a function of wire spacing. Shown in Fig. 10 is the change in inductance versus wire length. This information will allow optimization of amplifier performance during manufacture.

6. Wire Bonding

The ultrasonic bonding technique uses the transmission of ultrasonic energy under pressure to the bond interface. Bond quality can be determined by visual inspection of the deformed wire width.[4] When the deformed wire width is between 1.5 and 1.8 times the wire diameter, optimum bonding is achieved. Deformed widths greater than 1.8 are said to be "smashed" and are of poor quality since they yield low bond pull strength. The preferred method of optimizing the bond schedule is the pull test. In this test, the value of tensile strength is determined by hooking a gram gauge to the bonded wire and pulling until a break occurs. The wire diameter is chosen by current carrying capability and bonder limitations. A hard wire is suggested for a small diameter wire, $<50.8\ \mu m$, which translates to a tensile strength range of 15–19 grams for a $25.4\ \mu m$ diameter wire. The bond schedule is adjusted until reproducibility is achieved while high-bond strength is maintained. This procedure is of course a function of the wire bonder being used and also of operator skill and technique. Clamping pressure is used to hold the wire in contact with the bonding surface. Sometimes called the tool load, this force must be large enough to hold the wire in place without work piece movement and still be light enough to couple the ultrasonic energy into the bonding interface. The bond produced should then have the proper deformation.

Thermocompression bonding is a process using heat, pressure, and time to join the wire and work piece and results in a very strong bond. The one drawback is the high temperature required for the bond. The introduction of ultrasonic energy allows the reduction of temperature to 150°C from a pure thermocompression temperature of 350°C. Also called capillary bonding, this system is probably the most widely-used bonding technique in the industry today. Sometimes called ball bonding, this method uses a gold wire fed through a capillary bore. A hydrogen-fueled flame-off torch is used to melt the wire and cause a ball to be formed at the wire end. Thermocompression is then used to create the bond.

The bonding process we used is a combination of both thermocompression and ultrasonic energy and is sometimes called thermosonic

bonding. Initially, a ball bond is formed at the first wire position. The second connection is a wedge bond where, simultaneously, the wire is bonded and cut by forming a weak section and then pulling the wire away, creating what is called a tailless bond. This system allows a completely unassisted wire bonding operation.

7. Capacitors

Microwave applications require capacitors of very high Q and low inductance. A capacitor may be schematically represented as an ideal capacitance in series with an inductance and resistance.

The inductance depends on the physical characteristics of the component and the method of making the connection to the two capacitor pads. It is greatly reduced by planting the wire bond at the pad center instead of the pad end as is frequently done.

The resistance consists of losses of the dielectric and of the leads forming the connection. We define Q as the reciprocal of the dissipation factor (DF), $Q = \mathrm{DF}^{-1}$. At microwave frequencies, R becomes the principal source of loss and Q is

$$Q = \frac{X_c}{R}$$

The value of R increases dramatically with frequency, and for optimum amplifier performance must be addressed when selecting the capacitor manufacturer.

We employed the ATC 111 type capacitor* because it meets the small size requirement necessary for the program. Additionally, this capacitor has a very high Q (800), which is helpful in increasing the efficiency of high-current, low-impedance power amplifiers.

In the design selected, large inductors are attached to the capacitors causing the apparent capacity to be larger than the actual capacitance of the component.[3] The capacitance used is adjusted by

$$C = \frac{C_d}{C_d\,\omega^2 L + 1},$$

where C_d is the design capacitance value and L the series inductor value.

* American Technical Ceramics, Huntington Station, NY 11746.

8. Amplifier Optimization

A computer program was written to allow complete amplifier optimization at the point of manufacture. Optimization is performed by first measuring the completed amplifier S-parameters. The operator enters either S_{11} or S_{22} into the computer where the program will, by de-embedding sections of the circuit, re-compute the design. The measured capacitance and inductance are compared to the design values using either the standard FET data or the original S-parameter data of the device. From this information, a decision is made on a course of action to be taken. Three options are available: (1) if the wire is greatly oversized, replacement is the only alternative, 2) if the required inductance is in a range that can be adjusted by a parallel wire (from Fig. 9), this will be printed, and (3) where the capacitor has too low a value, tuning pads can be connected on the 50 Ω line to effectively bring it into range.

Sometimes both a parallel wire and tuning pads must be implemented. This occurs when a long wire is formed onto a capacitor having a value below the design value. The amplifier is remeasured after the changes have been made and again the computer program is used to evaluate the performance. When further improvement is no longer feasible, "no changes required" is printed out.

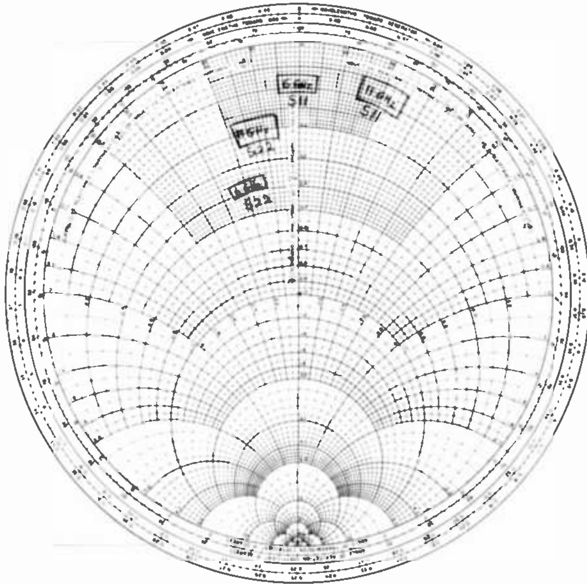

Fig. 11—Distribution of measured data at 6 and 11 GHz.

Table 7—Statistical Data from Measured S-Parameters

	Variance (σ^2)	Standard Deviation (σ)	Mean	Mean Deviation	Coefficient of Variation
At 6 GHz					
S_{11mag}	.0003	.0175	.8403	.014	2.0%
S_{11ang}	5.8	2.4	−177.0	2.07	1.4%
S_{22mag}	.0001	.0111	.4662	.009	2.4%
S_{22ang}	21.1	4.59	−155.5	3.9	3.0%
At 11 GHz					
S_{11mag}	.0009	.0308	.8628	.027	3.6%
S_{11ang}	9.7	3.11	159.2	2.6	2.0%
S_{22mag}	.0004	.0199	.6728	.015	3.0%
S_{22ang}	23.1	4.8	−165.6	3.9	3.0%

9. Device Parameter Range

Significant small-signal S-parameter data was collected from the 30 FET devices acquired for this program. Shown in Fig. 11 is the distribution of the measured data at 6 and 11 GHz. In Table 7, the associated statistical data are listed for the frequency end points. The distribution of the angles of S_{11} at 11 GHz, Fig. 12, shows that the elimination of just two data points will reduce the measured spread of values by nearly 37%. The distribution of phase angles of S_{11} data at 6 GHz, depicted in Fig. 13, falls more evenly across the window. The S_2 phase angle population at 6 GHz, shown in Fig. 14 is split between two bands of 2 and 5 degrees.

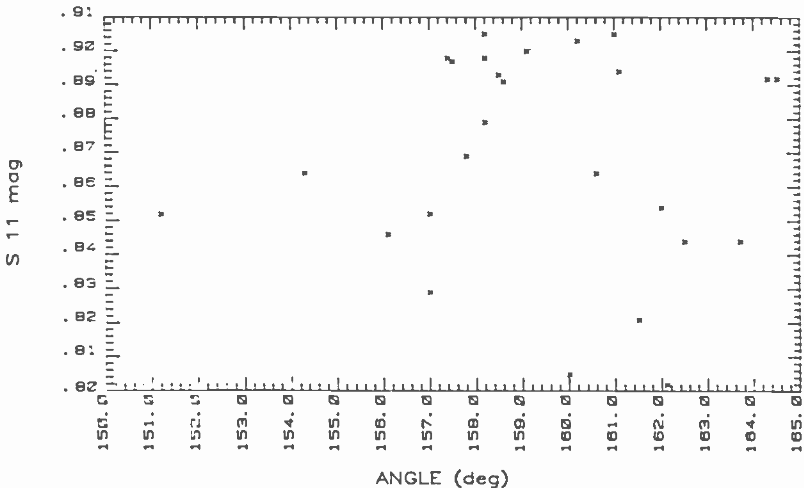

Fig. 12—Distribution of S_{11} at 11 GHz.

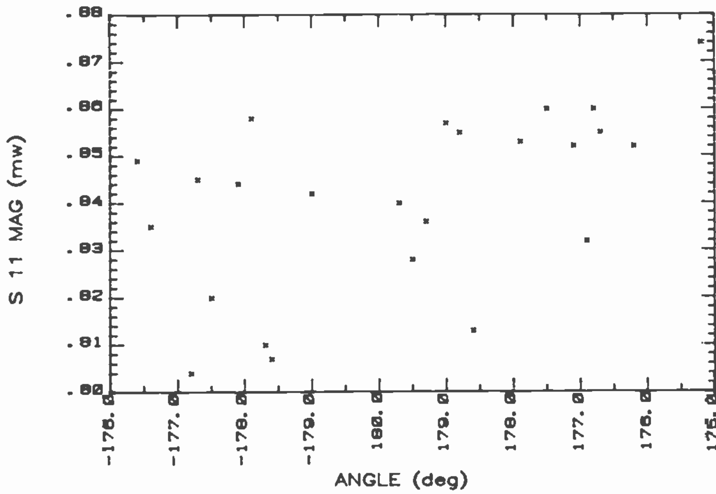

Fig. 13—Distribution of S_{11} at 6 GHz.

The spread of S_{22} at 11 GHz, in Fig. 15, also can be reduced by removing two data points.

The measure of relative variation allows us to compare the standard deviation of both magnitude and angle. We see by the coefficient of variation that our S-parameter measurements fall within a range of 2–3% from the mean value.

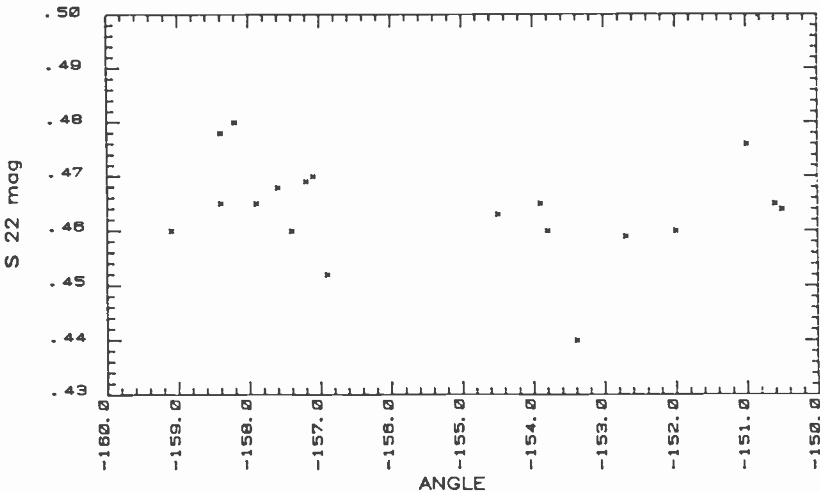

Fig. 14—Distribution of S_{22} at 6 GHz.

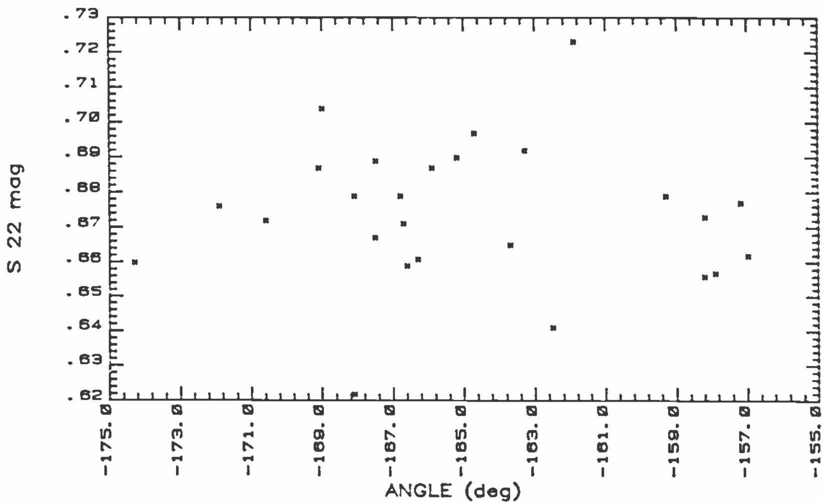

Fig. 15—Distribution of S_{22} at 11 GHz.

The ranges of inductor values needed to match all the devices are 0.093 nH for S_{11} and 0.1086 nH for S_{22}; the wire length changes required are 6 mils and 4.8 mils, respectively.

Conclusion

We have shown the feasibility of using wire bonds as inductors in a lumped-element power amplifier configuration. With wire bonding and automatic wire bonder construction, time is greatly reduced and inductor-to-inductor uniformity is maintained.

Techniques for trimming amplifier performance were developed and implemented with CAD and manual procedures. The time required for this very important trimming operation is greatly reduced and is eliminated altogether in many amplifiers by the close controls now established. Additionally, when trimming is required, it becomes a simple task with the aid of a computer program.

The device parameter spread should be approached with caution. We believe that all 30 devices received were produced from one GaAs wafer and processed together as one batch. It will take subsequent orders to gain a clear-cut picture of device-to-device variability. We now have, however, the knowledge to more fully specify the next purchase.

The area of performance requires that a minimum power gain be established below which either the amplifier is rejected or subjected to further trimming operations. A gain of 3 dB at 25 dBm input power is

presently being used. The power-added efficiency of the amplifiers fell into a range of 12–22% depending upon performance at frequency.

Acknowledgment

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Dual-Gate FET Phase Shifter*

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Abstract—A broadband dual-gate FET phase shifter that operates over the 4–8 GHz frequency band is described. The device is capable of continuous phase shift and a multiplicity of modulations, including (directly) digital phase shift and amplitude modulation and (indirectly, i.e., with additional informations processing circuits) single-sideband modulation, frequency modulation, and phase modulation. The dual-gate FET is used as a variable gain amplifier, and phase shift is obtained by complex addition of two orthogonal variable vectors.

The design, fabrication, and performance of components of the phase shifter that have been realized in monolithic and discrete form are presented. Although the dual-gate FET phase shifter described has been fabricated in MIC format on alumina substrates, the design is compatible with monolithic integration on GaAs substrates.

1. Introduction

In the past, ferrite phase shifters have been used in phased array radar systems. PIN diode phase shifters are now being considered because of their lighter weight, higher speed, and transmission reciprocity compared to the ferrites.[1-4] The ferrite and PIN diode phase shifters, however, both suffer from relatively slow response times. The recent interest in fully active phased array radars as well as progress in the monolithic GaAs integrated circuits has opened the possibility of active phase shifting subassemblies based upon GaAs field-effect transistors (FET).

The dual-gate FET has been used in many applications such as variable-gain amplifiers,[5] power limiters,[6] discriminators,[7] and mixers.[8] A single-frequency, dual-gate FET phase shifter has been reported.[9,10] The

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phase shift is obtained by changing the dc voltage applied to the control gate of the FET, and a linear phase shift of 100° has been obtained at a single frequency of 12 GHz. A phase shift of up to 140° was achieved using a three-device amplifier phase-shifter assembly.[11] Pengelly et al.,[12] studied the transmission phase variation of a gain-controlled, dual-gate GaAs MESFET amplifier at S-band, which depends upon the nature of the matching circuits used in the amplifier. These types of phase shifters are, in principle, capable of a relatively narrow bandwidth.

A narrow-band phase shifter has also been reported[4,13,14] in which the phase shift is obtained by complex vector addition of two orthogonal vectors. This circuit operates over a bandwidth of 1 GHz in the X-band. It is also possible to use three variable-gain amplifiers to obtain a 360° phase shift by using a vector sum of three non-orthogonal signals separated by 120° each.[15] This approach could lead to a small size, but is more suitable for narrow-band than for wideband applications.

This paper presents the design and development of an octave bandwidth, dual-gate FET phase shifter operating over the 4–8 GHz band, capable of a continuous phase shift from zero through 360°. The phase shift is obtained by the vector sum of four orthogonal signals whose amplitudes can be varied over a wide dynamic range. Four dual-gate FET amplifiers are used as variable-gain amplifiers for the amplitude control. The overall amplitude of the phase shifter can be varied by properly adjusting the gate voltages of the dual-gate FET amplifiers. Thus a signal of any phase and amplitude can be generated, and the phase shifter can be used as a vector generator. This phase shifter has been realized on a microstrip circuit, and is compatible with monolithic integration on a GaAs substrate.

The phase shifter reported here offers several advantages: (1) Minimal loss: because of the inherent high gain capability of the dual-gate FET, various signal processing such as switching and 180° phase inverting can be accomplished with very little loss; (2) Fast response: the response time of a dual-gate FET is of the order of a few hundred picoseconds. This fast response characteristic will lead to high-speed operation; (3) Capability of extending to a higher number of bits: the key element of the phase shifter is an analog 90° phase shifter employing two dual-gate FETs. It is feasible to increase the number of bits by changing the control voltages to the second gates; (4) Serrodyning for doppler shift can be readily performed; (5) The phase shifter has application in biphase modulation for secure communications or coding and beam steering.

The key component in the phase shifter is the dual-gate FET amplifier. The development of a truely monolithic dual-gate FET phase shifter—where all active and passive circuit elements or components and interconnections are formed into the bulk, or onto the surface of a

semi-insulating substrate—will require the integration of all the components of the phase shifter, i.e., 180° hybrid, 90° hybrid, dual-gate FET amplifier, and four-way, in-phase power combiner. We are in the process of developing these components in monolithic form. It is essential to design, fabricate and characterize the individual components before the final integration. We have developed a monolithic dual-gate FET amplifier,[16,17] monolithic interdigitated 90° coupler, 180° hybrid,[18] and four-way combiner.

This paper is divided in seven sections. In Sec. 2, the principle of operation of the phase shifter, design, fabrication and performance are described. Sec. 3 concerns the development of a monolithic dual-gate FET amplifier. Sec. 4 covers the design and fabrication and performance of the interdigitated 90° hybrid. In Sec. 5, the principle of a 180° hybrid, which has been designed and fabricated in planar form, is presented. Sec. 6 covers the design, fabrication and performance of a four-way, in-phase power combiner. The 180° hybrid and the four-way combiner are designed and fabricated in planar form on an Al_2O_3 substrate and are compatible for monolithic integration on a GaAs substrate. Progress in the development of the dual-gate FET phase shifter is summarized in Sec. 7.

2. Principle of Phase Shifter

2.1 90° Phase Shifter

The key element of the 360° phase shifter is an analog 90° phase shifter employing two dual-gate FETs. The conceptual design of the 90° phase shifter is shown in Fig. 1. The two dual-gate FET amplifiers are excited in quadrature phase through a hybrid power splitter at a designated rf frequency. The outputs of both FET amplifiers are then combined through an in-phase power combiner to produce a phase-controlled output. The two dual-gate FET amplifiers are used as variable gain amplifiers.[5] The gain of a dual-gate FET amplifier can be controlled from +10 dB to −30 dB (cut off) by controlling the second gate bias voltage.[5] The phase difference in path A and path B (Fig. 1) is 90°. The resulting vector sum of the two combined quadrature rf signals is given by:

$$\mathbf{C} = \mathbf{A} + \mathbf{B} \qquad [1]$$

$$C\angle\phi = A + jB = |C|\angle\tan^{-1}B/A \qquad [2]$$

where C is the resultant rf voltage amplitude and ϕ is the phase angle. The output phase angle is, therefore, controlled by adjusting the relative amplitudes of the quadrature vectors **A** and **B**. This is accomplished by

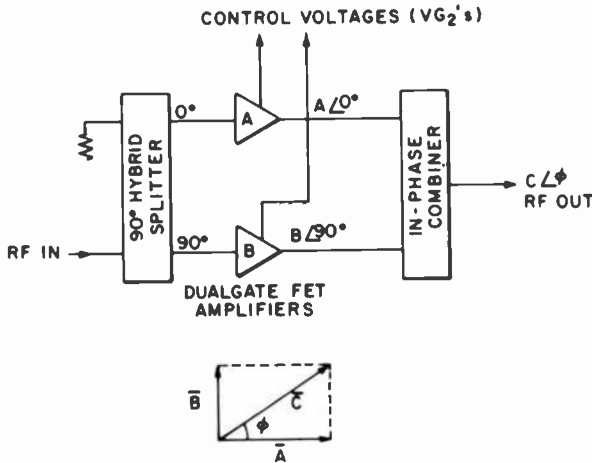


Fig. 1—Schematic of a 90° GaAs dual-gate FET phase shifter.

independently adjusting the gain of each of the dual-gate FET amplifiers.

For most system requirements, the absolute amplitude of the resulting phase shifted rf signal must be kept constant, independent of the selected output phase angle. This means that C is invariant and the phase angle is selected by controlling the amplitudes of both rf signals, A and B. For this unique requirement

$$\sqrt{A^2 + B^2} = \text{constant}. \quad [3]$$

This can be obtained by partially biasing amplifiers A and B so that the output is at the 0.707 level. The overall amplitude of the phase shifter can be varied by changing the gate voltages of both amplifiers simultaneously. Thus in Eq. [3], the constant output amplitude level can be varied and this phase shifter becomes a vector generator. A vector generator is a device where a vector of any phase or amplitude (with respect to an input reference signal) can be generated.

2.2 360° Phase Shifter

Fig. 2 illustrates the schematic of a continuously variable 0° to 360° phase shifter. The 360° phase shift is achieved by the sum of four quadrature vectors $A\angle 0°$, $B\angle 90°$, $C\angle 180°$, and $D\angle 270°$ with properly controlled amplitudes of A, B, C, and D. Those four quadrature vectors can be realized by a 180° power divider, two 90° hybrids, four dual-gate FET amplifiers, and an in-phase, four-way power combiner, as shown in Fig. 2.

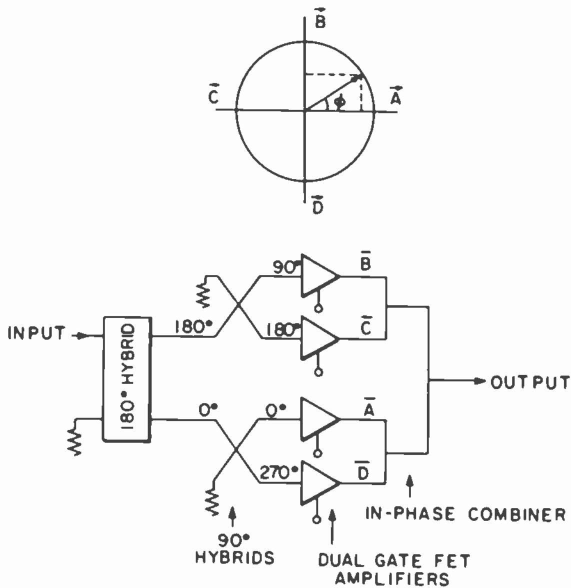


Fig. 2—Schematic of a 360° GaAs dual-gate FET phase shifter.

The incoming signal is first divided into two signals equal in amplitude but 180° apart in phase. Then each signal is further divided into two signals through a 90° hybrid, resulting in four signals of equal amplitude and having phases of 0°, 90°, 180°, and 270°. Each signal is then amplified through a dual-gate FET amplifier, and the four outputs are then combined through a four-way, in-phase combiner to obtain a phase-controlled output. Fig. 2 illustrates the four quadrants of 360° phase shift that are obtained using a combination of two vectors at a time.

Each dual-gate FET serves as an amplifier-switch that can control the amplitudes of the vectors **A, B, C,** and **D**. For example, when **C** and **D** are switched off and **A** and **B** are switched on, an output signal with about 30° phase advance relative to the input signal is obtained (Fig. 2). By changing the second-gate bias voltages of amplifiers A and B (when C and D are switched off), the total 0° to 90° phase shift can be obtained. Thus by controlling the bias voltages of two amplifiers at one time, while the other two are switched off, the total of 360° continuous phase shift is obtained.

It is appreciated that,

$$\omega = \frac{d\phi}{dt}. \qquad [4]$$

Thus by applying varying potentials to the control gates, the phase can

be continuously rotated at a given rate resulting in an output frequency offset in frequency from the input frequency. It can be shown that by proper choice of input signals to the four control gates, the following modulation functions may be performed:

(a) Amplitude modulation
(b) Pulse code modulation
(c) Frequency modulation
(d) Phase modulation
(e) Continuous phase modulation
(f) Bi-phase shift keying
(g) Quadra-phase shift keying
(h) Multi-phase shift keying
(i) Single-side-band modulation
(j) Combination of above

2.3 Design, Fabrication and Performance of the Phase Shifter

The deisgn of the 360° phase shifter includes the 180° hybrid, 90° hybrid, four-way combiner, and dual-gate FET amplifier. The design, fabrication and performance of the 180° hybrid, 90° hybrid and four-way, in-phase combiner are presented in Secs. 4, 5, and 6, respectively. The dual-gate FET amplifier design is done using CAD techniques,[5] using the NEC 46 300 dual-gate FET. Fig. 3 shows the variation of gain with frequency

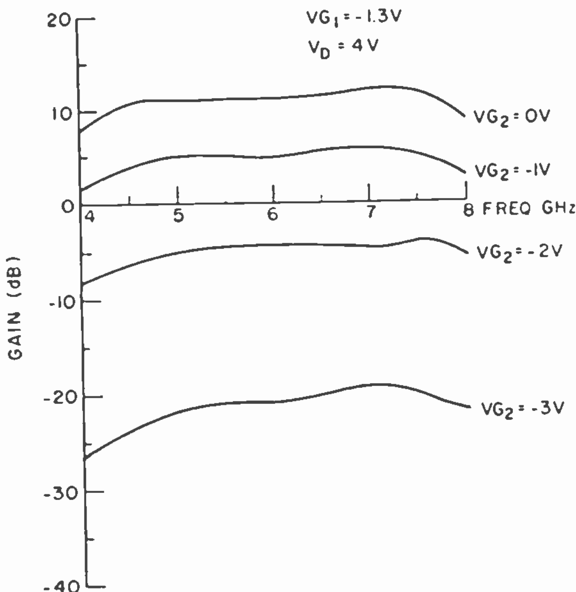


Fig. 3—Variation of gain versus voltage (V_{G2}) of a dual-gate FET amplifier.

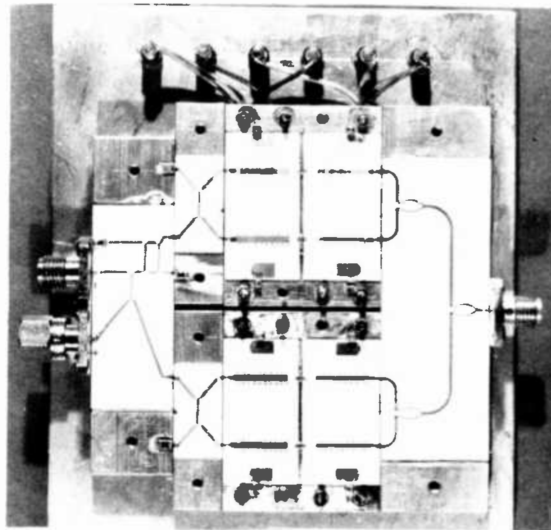


Fig. 4—Photograph of the 360° phase shifter.

for different second-gate bias voltages. The gain of the amplifier can be varied from 10 dB to −30 dB (cut-off) by changing the second-gate (control gate) bias voltage.

Fig. 4 is a photograph of the 360° phase shifter. All the passive circuit components, such as the 90° and 180° hybrids, Wilkinson four-way combiner and dc bias circuits of the dual-gate FETs, are designed in planar form so that the complete phase shifter can readily be integrated on a monolithic GaAs chip.

Fig. 5 shows the variation of phase shift with control voltages (second-gate bias voltages). The 0° to 360° continuous phase shift is obtained

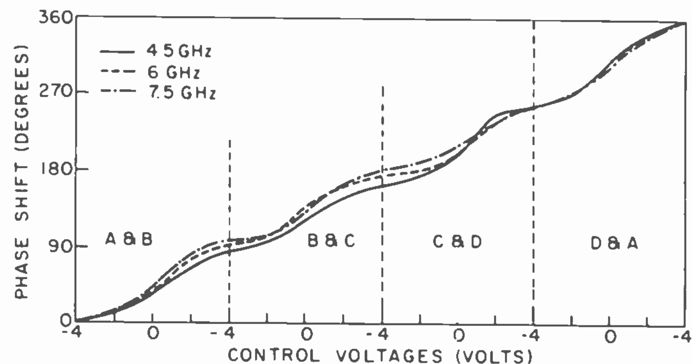


Fig. 5—Variation of phase with control voltages of 360° phase shifter.

by changing the second-gate bias voltages of the dual-gate FET amplifiers in a systematic manner. In Fig. 5, there are four sections which divide the total phase shift of 360°. Each section represents the phase control of one quadrant. In each quadrant, the control voltages of two dual-gate FET amplifiers are varied, while the remaining two amplifiers are switched off by applying −4 volts to their second gates.[5] For example, in the first quadrant, the V_{G2}'s for A and B are varied while the V_{G2}'s for C and D are kept at −4 volts. To get a 90° phase shift, amplifier A is kept in the *on* condition ($V_{G2}(A) = 0$ volts), and $V_{G2}(B)$ for amplifier B is varied from −4 volts to 0 volts, which gives approximately 45° phase shift (Fig. 5). Next, amplifier B is switched on ($V_{G2}(B) = 0$ volts) and the $V_{G2}(A)$ for amplifier A is varied from 0 to −4 volts, which gives approximately from 45° to 90° phase shift. Thus controlling the two second gate bias voltages of two amplifiers provides a 90° phase shift. This process is repeated with other combinations of two orthogonal vectors to obtain the entire 0° to 360° phase shift.

The variation of amplitude with phase is presented in Fig. 6. The gain of the phase shifter is plotted as a function of phase for different frequencies. The maximum variation of gain is ±3 dB for a 360° phase shift. As explained earlier, the phase shift at 0°, 90°, 180°, and 270° is obtained by switching three amplifiers *off* while leaving only one amplifier *on*; this gives a variation of 5 dB in amplitude because of the four-way power combination characteristic.[19,20] It is possible to achieve a constant output power for any given phase by partially biasing two amplifiers instead of biasing only one amplifier at a time and keeping others off.[21]

3. Development of Monolithic Dual-Gate FET Amplifier

One of the major concerns in the development of monolithic microwave integrated circuits is the long iteration time required before the final

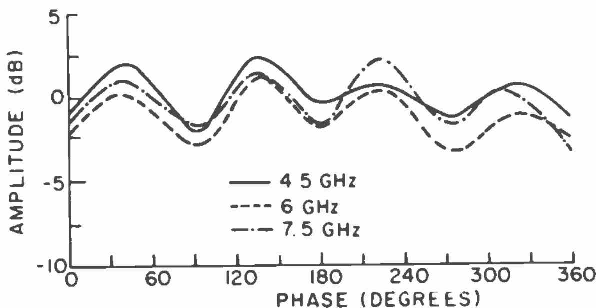


Fig. 6—Variation of amplitude with phase of 360° phase shifter.

design is completed. There are a number of variations that cannot be predicted with sufficient accuracy for normal circuit design techniques to perform satisfactorily. These variations can result from the lumped-circuit-element values, from the material characteristics, and from the physical dimensions. Because of these considerations, we have designed a monolithic dual-gate FET amplifier endeavoring to minimize performance sensitivity to the circuit variations.

The monolithic dual-gate FET amplifier was designed, using lumped circuit elements to operate over 4–8 GHz. A computer-aided design technique was employed to obtain the optimal circuit approach and to perform a sensitivity analysis of each matching element. Each element was varied by ±10 percent of its nominal value and its effect on gain of the amplifier was analyzed. The circuit diagram of the amplifier is shown in Fig. 7. This circuit approach showed a 0.5-dB gain variation over the band with ±10-percent variations in all the element values.

The fabrication of monolithic dual-gate FET amplifiers begins with an n^+-n-semi-insulating GaAs wafer. The nominal carrier density of the active layer is 1×10^{17} cm^{-3} and that of the n^+ layer is 1×10^{18} cm^{-3}. Each epitaxial layer is nominally 0.5 μm thick. A variation of the anodic thinning process[22] is used to thin the active channel areas to the "pinchoff" thickness while leaving n^+ material in the source and drain regions. Individual devices are then isolated using a citric acid etchant[23] to produce the mesa region. Ohmic contacts are produced by the liftoff of AuGe/Ni (1500 Å/500 Å) and sintering at 450°C for 60 s.

Prior to defining the gates in photoresist, the device channels are chemically etched to adjust the saturation current, and a 0.1-μm-thick layer of titanium is deposited uniformly across the wafer. This titanium layer serves to improve the adhesion of the gate metallization and as a conduction path for Au plating. The nominal 1.5-μm-long gates and matching element components are next defined in photoresist for the liftoff of Ti/Pt/Au metallization approximately 0.5 μm thick. Liftoff is again used to increase the metal thickness on the ohmic contacts by depositing Ti/Pt/Au. After liftoff, the matching elements are redefined

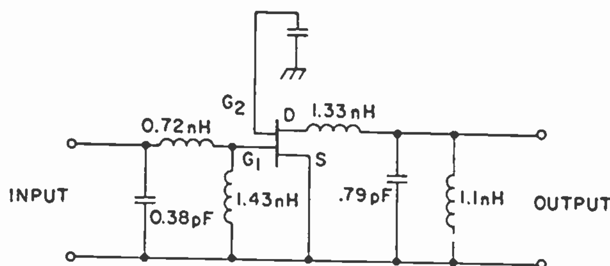


Fig. 7—Circuit diagram of GaAs monolithic dual-gate FET amplifier.

in thick photoresist (8–10 μm) and plated with 6–7 μm of gold. After careful solvent cleaning, the titanium layer is chemically etched away with an etchant containing HF, HNO_3, and H_2O.[24] Fig. 8 shows the monolithic amplifier chip. The unit gate width is 150 μm. The length of the first and second gates is 1.5 μm. The separation between the first and the second gate is 3 μm and the source-to-drain spacing is 9 μm.

Fig. 9 shows the gain of the amplifier as a function of frequency over the 4–8 GHz band. The preliminary results show that a gain of 3.5–5 dB is obtained over the band with the second gate grounded. This gain is achieved without any trimming of the circuit elements.

4. Development of Monolithic Interdigitated 90° Coupler

A monolithic 90° hybrid is an important and very useful passive component for MMIC (monolithic microwave integrated circuit) applications such as balanced amplifiers, mixers, discriminators, and phase shifters. The recently reported monolithic interdigitated 90° coupler on GaAs substrates has been designed and fabricated with conventional input- and output-impedances of 50 ohms.[25-27] The thickness of GaAs substrates used for most applications is 0.1 mm. The width and spacing of the interdigitated conductors are 6.5 and 7.0 μm, respectively. The conductor losses are reduced by more than a factor of two if the width and spacing are doubled by increasing the thickness from 0.1 to 0.2 mm.

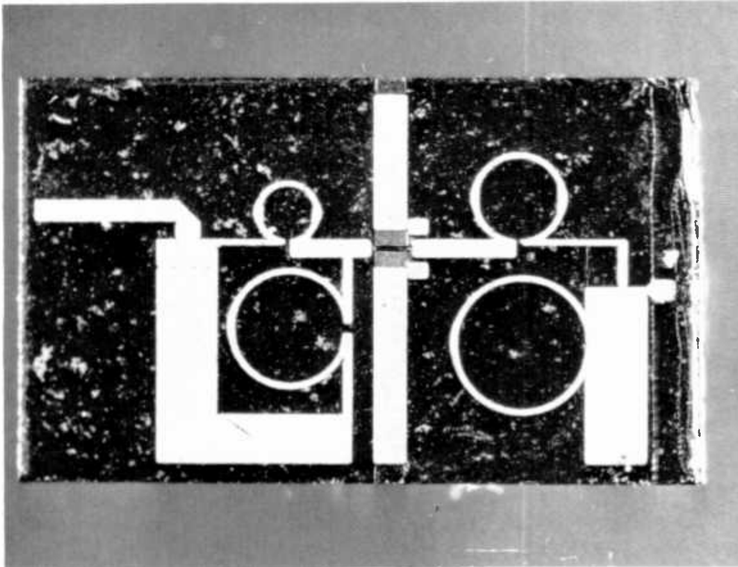


Fig. 8—Photograph of the GaAs monolithic FET amplifier.

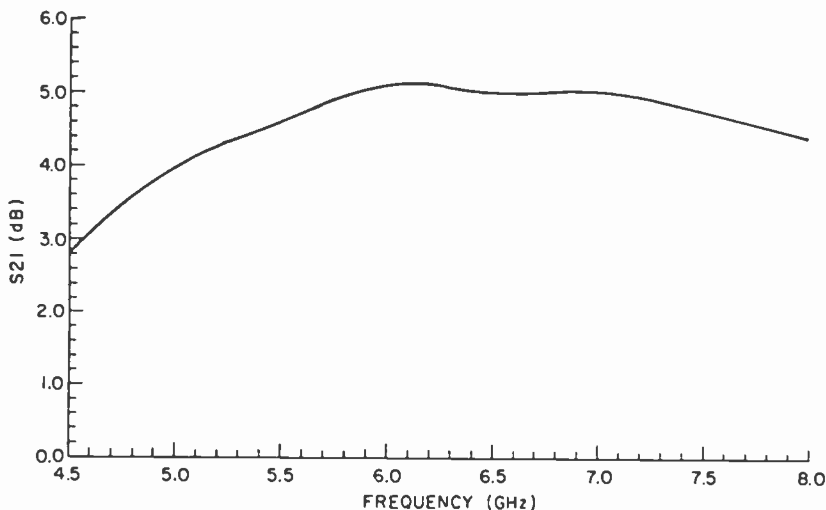
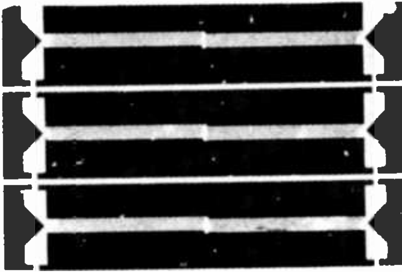


Fig. 9—Gain as a function of the GaAs monolithic dual-gate FET amplifier.

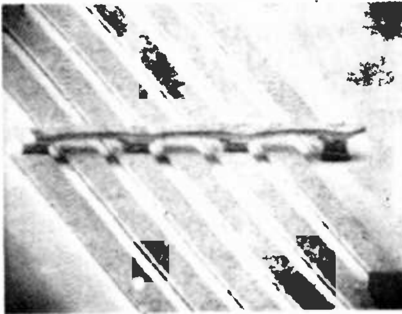
However, thermal resistance, electrical performance, and fabrication technology have dictated the choice of 0.1-mm-thick substrates for all MMIC applications.

The input- and output-impedances of a GaAs power FET are on the order of a few ohms. For most applications in MMICs these input- and output-impedances have to match the coupler's impedance, generally 50 ohms. To overcome such a large mismatch (from a few ohms to 50 ohms), multi-section matching networks have to be used. This leads to high loss in the matching networks and a relatively large matching network which consumes a large area of GaAs real estate. By using a coupler having a lower impedance than 50 ohms, the matching circuits will require fewer matching elements, resulting in savings in the GaAs substrate area and in reduced loss in the matching circuits.

A 6-line coupler is preferred to a 4-line coupler. The spacing between the interdigitated conductors is 4.3 and 11.0 μm for 4-line and 6-line couplers, respectively. Thus, the 6-line coupler has the advantage of smaller fabrication tolerance and low loss. The coupler has been fabricated on a 0.1-mm thick GaAs semi-insulating substrate. The line width and gap are 19.0 and 11.0 μm, respectively. A photograph of the coupler is shown in Fig. 10. The coupler performs well over an octave band in C-band. The average insertion loss of the coupler is 0.3 dB (compared with 0.5–0.7 dB for a 4-line, 50-ohm coupler). The isolation between two output ports is better than 18 dB over the band. The measured results of coupling and insertion loss are presented in Fig. 11. As can be seen, the performance of this monolithic coupler on GaAs substrates is compatible to that on Al_2O_3 substrates.



(a)



(b)

Fig. 10—Photograph of the monolithic interdigitated 90° coupler: (a) 6-line coupler structure; (b) SEM micrograph of air bridge.

Air-bridge interconnections were used to minimize the cross-over capacitance. The coupler was tested on a 50-ohm system using a 25- to 50-ohm $\lambda/16$ four-section transformer. The results presented in Fig. 11 do not include fixture loss.

5. Development of 180° Hybrid

In the past, 180° hybrids have been extensively used in balanced mixers, switching networks, phase shifters, and push-pull amplifiers. The recent interest in monolithic GaAs integrated circuits has opened the need for a 180° planar hybrid compatible with monolithic integration on GaAs substrates.

Conventional hybrid rings have been used as 180° hybrids. The hybrid ring has a narrow bandwidth. Reflection-type, 180° hybrids have been

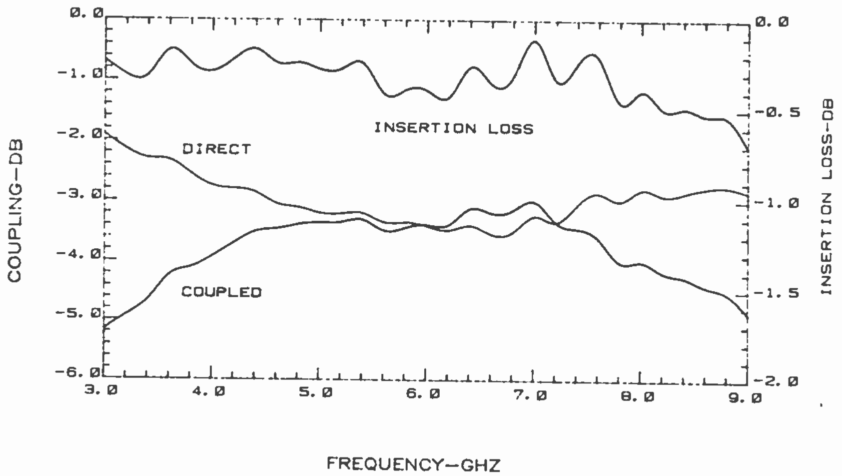


Fig. 11—Coupling and insertion loss variation with frequency of an interdigitated 90° coupler.

reported.[28] The problem with these hybrids is the practical difficulty of realizing a good short or open-circuit over a wide band of frequencies. Commerically available 180° hybrids have a tandem connection of two couplers using broadside coupling.[29,30] This is a multi-layer structure and can be realized using striplines only. Recently a 3-dB, 180° hybrid has been reported[31] that uses a slot line-microstrip coupling. The above-mentioned structures for 180° hybrids are not planar and are not very compatible with monolithic circuit fabrication.

This section presents an analysis and experimental results of a broadband, 180° planar hybrid. This hybrid is a 4-port device with two input ports and two output ports. One of the input ports is designated as the sum port and the other as the difference port. A signal fed into the sum port or the difference port is divided into two signals of equal amplitude with a phase difference of 0° or 180°, respectively. This hybrid has been realized using a 3-dB interdigitated 90° hybrid and a 0-dB 90° interdigitated tandem hybrid.[32] The latter introduces an additional 90° phase shift independent of frequency. The analysis of the circuit is presented. The hybrid has been designed and fabricated on an alumina substrate for C-band operation.

5.1 Analysis of the Hybrid

The schematic of the hybrid is shown in Fig. 12. It is a four-port device. Ports 1 and 2 are the input ports and ports 3 and 4 are the output ports. When the signal is fed to port 1, the signals appearing at port 3 and port 4 are both 3 dB below the input signal and have a phase difference of

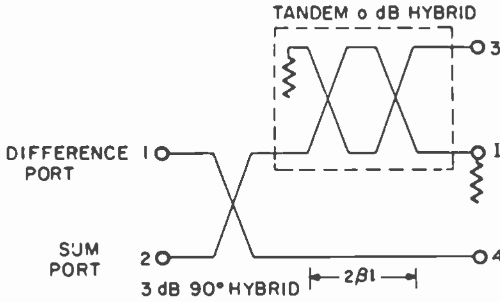


Fig. 12—Schematic of a 180° hybrid.

180°. When a signal is fed at port 2, the signals appearing at ports 3 and 4 are both 3 dB below the input signal and are in phase. These two cases are considered separately and the analysis is presented for both cases.

We first analyze the 3-dB, 90° hybrid and the tandem 0-dB coupler. Fig. 13(a) shows the 90° hybrid. Let θ be the coupling angle and l be the coupling length. Assume that a unit amplitude signal is fed at port 1 (when port 2 is terminated), then the amplitudes of the signals appearing at ports 3 and 4 are

$$\text{Signal at port 3} = j \sin\theta e^{-j\beta l} \quad [5]$$

$$\text{Signal at port 4} = \cos\theta e^{-j\beta l}, \quad [6]$$

where β is the propagation constant. If a signal is fed at port 2 when port 1 is terminated, the signals appearing at ports 3 and 4 are given by Eqs. [6] and [5], respectively.

Fig. 13(b) shows a schematic of a tandem connection of two 3-dB, 90° hybrids. Again, θ is the coupling angle and l is the coupling length for each hybrid in the tandem coupler. Assume that a unit amplitude signal is fed at port 1 (when port 2 is terminated), then the signals appearing at ports 3 and 4 are

$$\text{Signal at port 3} = j \sin 2\theta e^{-j2\beta l} \quad [7]$$

$$\text{Signal at port 4} = \cos 2\theta e^{-j2\beta l}. \quad [8]$$

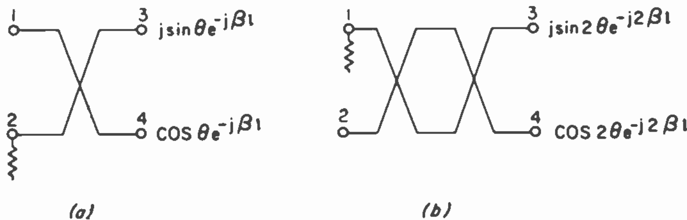


Fig. 13—Analysis of hybrid: (a) 90° hybrid, (b) tandem hybrid.

If the signal is fed at port 2 (when port 1 is terminated), the signal at ports 3 and 4 is given by Eqs. [8] and [7], respectively.

Case 1: Input at Difference Port

In the hybrid illustrated in Fig. 12, port 4 has an extra transmission line length of $2\beta l$. It will be shown later that the phase difference of the two output signals appearing at ports 3 and 4 is independent of frequency. Assume that a unit amplitude signal is fed at port 1 (port 2 is theoretically isolated), then the signals appearing at ports 3, 4, and I can be obtained as

$$\text{Signal at port 3, } V_3 = -\sin\theta \sin 2\theta e^{-j3\beta l} \quad [9]$$

$$\text{Signal at port 4, } V_4 = \cos\theta e^{-j3\beta l} \quad [10]$$

$$\text{Signal at port I, } V_I = j \sin\theta \cos 2\theta e^{-j3\beta l}. \quad [11]$$

For $\theta = \pi/4$ at band center, for a 3-dB hybrid, Eqs. (9)–(11) become

$$V_3 = -0.707\, e^{-j3\beta l} \quad [12]$$

$$V_4 = 0.707\, e^{-j3\beta l} \quad [13]$$

$$V_I = 0. \quad [14]$$

Thus, the signals appearing at ports 3 and 4 have a phase difference of 180° and are equal in magnitude which is $\sqrt{2}$ below the input signal (3 dB below in power). Port I is an isolated port since the signal appearing at that port is zero.

Case 2: Input at Sum Port

In this case the signal is fed at port 2 (Fig. 12) and port 1 is theoretically isolated. The signals appearing at ports 3, 4, and I can be obtained as

$$\text{Signal at port 3, } V_3 = j \cos\theta \sin 2\theta e^{-j3\beta l} \quad [15]$$

$$\text{Signal at port 4, } V_4 = j \sin\theta e^{-j3\beta l} \quad [16]$$

$$\text{Signal at port I, } V_I = \cos\theta \cos 2\theta e^{-j3\beta l}. \quad [17]$$

For $\theta = \pi/4$ at band center for a 3-dB hybrid, Eqs. [15]–[17] become

$$V_3 = j\, 0.707\, e^{-j3\beta l} \quad [18]$$

$$V_4 = j\, 0.707\, e^{-j3\beta l} \quad [19]$$

$$V_I = 0. \quad [20]$$

Thus signals appearing at ports 3 and 4 are in phase and of equal amplitude, each 3 dB below the input power. Port I is an isolated port and is match terminated.

In both cases, the phase difference between two output ports is in-

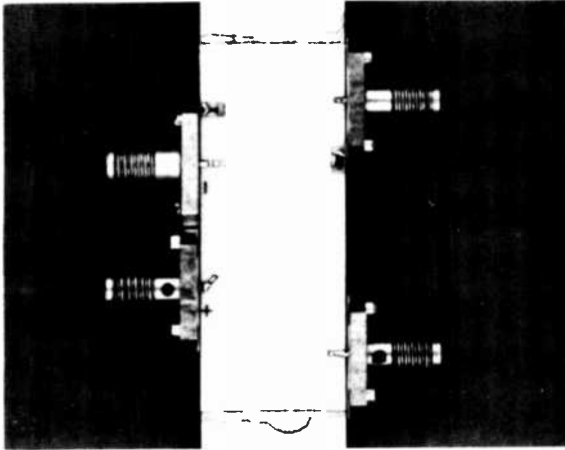


Fig. 14—Photograph of the 180° hybrid.

dependent of frequency. However, the amplitude is frequency dependent, since the coupling angle θ is frequency dependent.The bandwidth of the hybrid will be slightly less than the bandwidth of each 90° hybrid used. A 90° interdigitated hybrid has over an octave bandwidth.

5.2 Experimental Results

The hybrid shown in Fig. 12 consists of three 3-dB 90° hybrids. The design of an interdigitated 90° hybrid is done using well-documented theory.[33,34] We have fabricated this hybrid on a 0.0635-cm thick alumina substrate as shown in Fig. 14. Fig. 15 shows the coupling between different ports of the hybrid. The isolation between two output ports is better than 18 dB. The powers of the two output ports differ by less than 1.5 dB and the insertion loss of the hybrid is less than 0.5 dB over the 4–8 GHz band. The variation of the phase with frequency is presented in Fig.

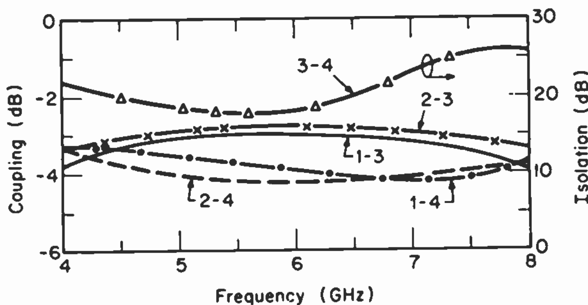


Fig. 15—Coupling and isolation between different ports versus frequency of the hybrid.

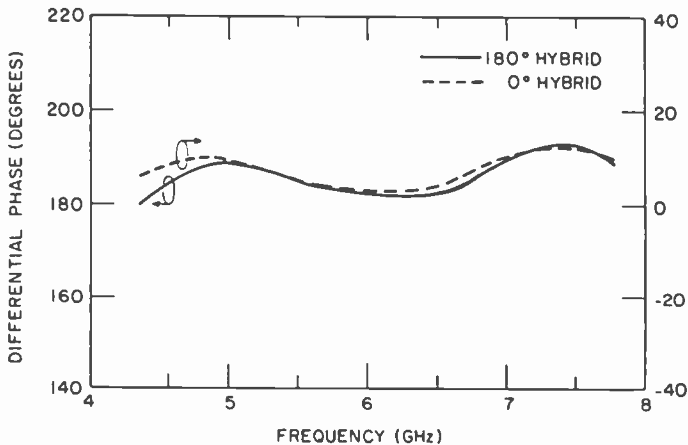


Fig. 16—Differential phase versus frequency for 180° and 0° hybrids.

16 for both cases, i.e., when the signal is fed at the difference port or sum port, resulting in the two output signals either being 180° out of phase or in phase. The maximum VSWR at the difference port is 1.4 over the band.

6. Development of Four-Way Power Combiner/Divider

We have developed a planar, four-way, in-phase power combiner/divider. Though the combiner/divider has been fabricated on alumina substrate, the design and its planar structure are compatible with monolithic integration on GaAs substrates and with other passive and active components. The schematic of a planar, four-way, in-phase power combiner/divider is shown in Fig. 17. The input is split into four outputs through four $\lambda/4$ sections of the transmission lines. The impedance of each $\lambda/4$ section of line is 100 Ω,[35] and the value of the isolation register is 70.7 Ω. The input and output impedances are 50 Ω each. The com-

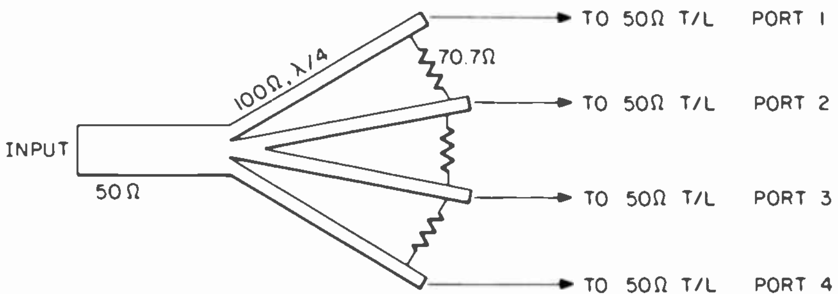


Fig. 17—Schematic of planar four-way power divider/combiner.

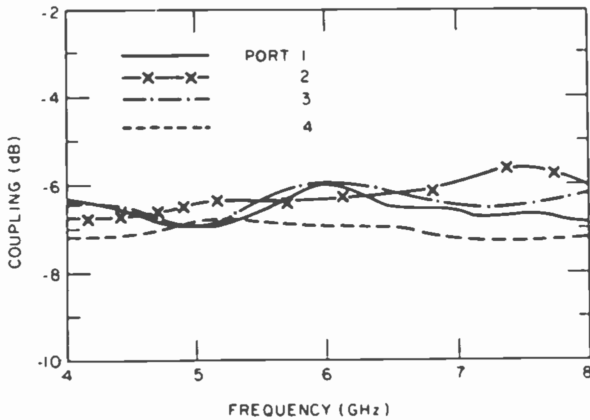


Fig. 18—Variation of coupling with frequency.

biner/divider was fabricated on a 0.0635-cm thick alumina substrate. The performance of the combiner/divider is shown in Figs. 18 through 21. Fig. 18 shows the variation of coupling at four output ports with frequency. Fig. 19 presents the isolation versus frequency between any two output ports, which is better than 13 dB over the band. The insertion loss and return loss of the combiner/divider are presented in Figs. 20 and 21, respectively. The overall phase variation between signals at the output ports is ±6°.

Summary

A broadband active phase shifter using dual-gate FETs operating over the 4–8 GHz band has been described. Continuous 360° phase shift is

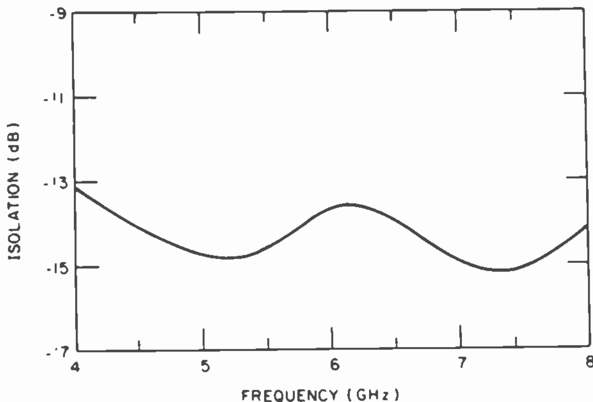


Fig. 19—Variation of isolation betweeen ports with frequency.

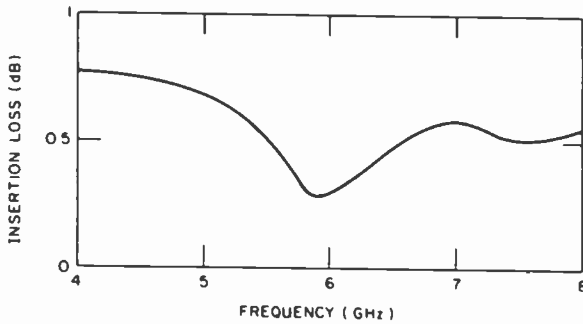


Fig. 20—Variation of insertion loss with frequency.

obtained with minimal loss. The phase shifter has several advantages over the other kinds of phase shifters—light weight, fast response, low loss, and octave bandwidth capability.

The phase shifter design presented here is compatible with monolithic integration on GaAs substrates. The 180° hybrid and in-phase combiner have been designed and fabricated in planar form and are compatible for monolithic integration on GaAs substrates with other passive and active components of the phase shifter. The dual-gate FET amplifier and 90° interdigitated hybrid have been designed and fabricated in monolithic form. The technology has been established for monolithic integration of all the components of the phase shifter. Work on development of the monolithic phase shifter is continuing.

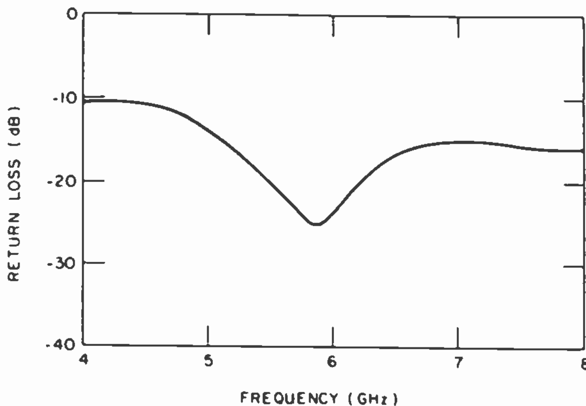


Fig. 21—Variation of return loss with frequency.

Acknowledgments

The author wishes to thank H. Huang for his encouragment and helpful discussions. The contributions of G. C. Taylor, S. N. Subbarao, and R. J. Menna are gratefully acknowledged. Thanks are also due to E. Mykietyn and P. A. Czajkowski for assistance in the assembly of the phase shifter.

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A Ku-Band Continuously Variable Phase/Amplitude Control Module

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Abstract—A Ku-band microstrip phase shifter capable of continuous phase and amplitude control is described. Three dual-gate FET amplifiers provide variable amplitude vectors that are separated by 120° and summed through an arrangement of quadrature couplers. The described phase shifter provides a full 360° shift with an amplitude weighting capability of more than 20 dB.

Introduction

An increasing number of electronic warfare applications exist for adaptive phased arrays having tight illumination tolerances for both shaped and low-side-lobe beams. As these tolerances decrease, the phase and amplitude setting accuracy of each radiating antenna element or section must correspondingly increase.

There are two basic types of phase shifters for this job. those that step incrementally through the phases and those that provide continuous phase tuning. Discretely stepped phase shifts using PIN switches or varactor diodes can cover a full 360° by cascading a series of phase shifting sections, each section having the capability of "switching in" twice the incremental phase shift of the preceding sections. A stepped phase shifter with N sections, or bits, is therefore capable of $360/2^N$ degrees per phase step. A minimum of one and typically two active devices are required for each section.

A relatively high phase setting accuracy of, say, 10° requires at least a 5-bit phase shifter. This results not only in a large parts count but, more

importantly, puts very stringent requirements on the allowable phase error of each section, since the overall error is the cumulative error of the 5 cascaded sections. This phase shifter type is therefore only practical for low bit numbers.

A circuit having an adjustable gain must also be added if amplitude weighting is required. Continuous phase and amplitude control has the advantage over the discretely stepped approach of attaining any desired setting accuracy. Another more important advantage is the capability of continuous control to compensate for variations in circuit path length, or losses, which is a serious problem at frequencies above X-band. This compensation can be made through the use of recently developed automated near-field measurements. One type of continuous phase shifter uses ferrite structures immersed in a variable magnetic field that changes the phase through the circuit. However, these structures are bulky and have long response times and high control power requirements, making them unsuitable for many phased array applications.

A second general type that has been described in the literature, uses dual-gate FET amplifiers[1] or variable PIN attenuators[2] to control the vector amplitudes in a vector-summing arrangement.[3] The PIN attenuator phase shifter has the advantage of reciprocity, while the dual-gate FET approach has lower insertion loss and faster tuning response with lower associated control power requirements.

Each of the vector-summing type circuits have included four or more active devices requiring control of each device. This paper describes a potentially compact phase/amplitude control module using only three dual-gate FET devices.

General Design Considerations

In previously reported continuously variable phase shifters, the full 360° shift is obtained by vector manipulation of four vectors, with the vector angular separation being derived from mixers, PIN switches, or quadrature couplers. Any number of vectors, N, greater than 2 can be used. Only two vectors, of variable amplitudes A_1 and A_2 and separated by angle θ, are necessary to provide a resultant vector of amplitude A at angle ϕ, within θ (see Fig. 1):

$$A = \tan^{-1} \frac{A_2 \cos\left(\theta - \frac{\pi}{2}\right)}{A_1 - A_2 \cos(\pi - \theta)},$$

$$\phi_1 = (A_1^2 + A_2^2 - 2A_1A_2 \cos\theta)^{1/2}. \qquad [1]$$

The maximum attainable constant-amplitude-versus-phase vector

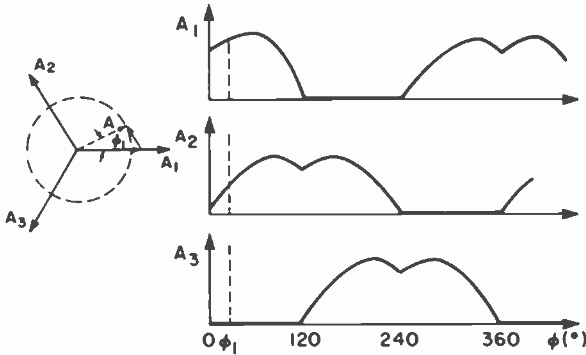


Fig. 1—Three-vector phase and amplitude control diagram.

is strongly dependent on the component vector angle separation θ. The voltage of the resultant vector varies as $\sin\theta$.

For N equal to three or four, the optimum component vector angular spacing is $2\pi/N$, since for any two-vector spacing less than $2\pi/N$ there exists a vector spacing greater than $2\pi/N$ having a corrresponding reduction in the resultant vector amplitude. For N greater than four, the maximum attainable constant-amplitude-versus-phase vector equals the smallest component vector amplitude for any two-vector spacing, θ, of $\pi/2$ or less.

A phase shifter using only three vectors has the advantages of lower parts count and, ultimately, smaller size and lower cost. Fig. 1 shows the respective vector amplitudes for the three-vector case necessary to obtain any desired resultant phase with constant amplitude. The 120° vector separation can be achieved by adding 30° transmission line lengths to the quadrature coupler outputs, as shown in Fig. 2. The vector ampli-

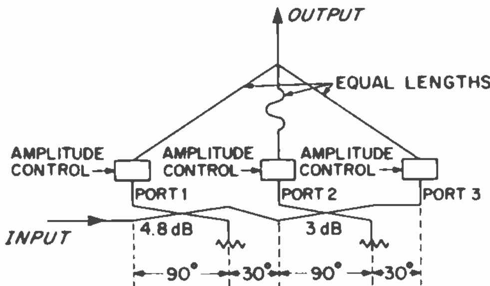


Fig. 2—Phase shifter using in-phase direct combiner.

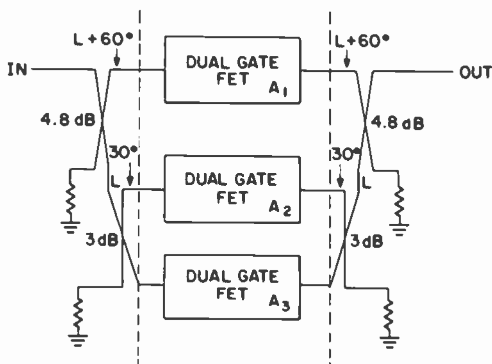


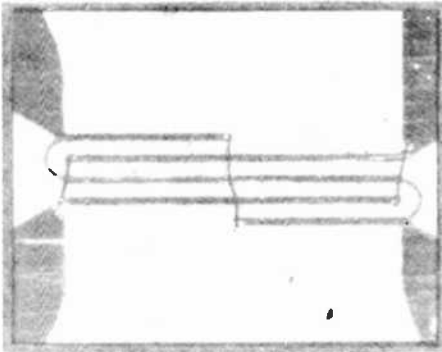
Fig. 3—Continuous phase and amplitude control.

tudes are controlled by the variable gain amplifiers whose outputs are combined in-phase.

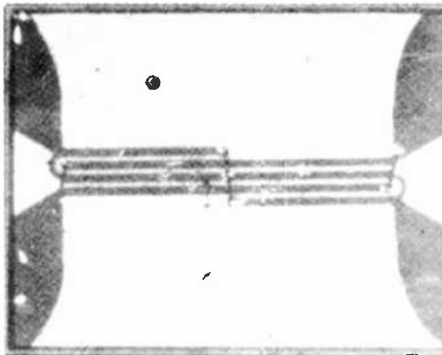
Circuit Description

For the first experimental unit we selected the symmetrical circuit configuration shown in Fig. 3. In this arrangement, the power from the direct port of a 4.8-dB quadrature coupler is further divided by a 3-dB quadrature coupler[4,5] to provide the three equal power inputs to the amplifiers. The interconnecting line lengths are chosen to provide 60° output separation. Each of the three transmission paths includes the same number of right angle bends to help maintain phase tracking. A mirror image of the coupler assembly is used to combine amplifier outputs and to add the additional 60° separations for the 0°, 120°, and 240° vectors. The 3- and 4.8-dB coupler designs were constructed on 15 mil alumina and are shown in Fig. 4. Two of the six interconnecting wires were replaced by printed lines extending around the ends of the couplers. This was done to simplify the construction of future couplers where the remaining four interconnections will be replaced by thin-film metal bridges. The coupler configuration shown in Fig. 5 was fabricated with an additional equivalent length of 50-ohm line so that coupling losses could be separated from the transmission line loss. The performance of the 3- and 4.8-dB couplers is shown in Figs. 6 and 7.

The 50-ohm-line loss measures approximately 1 dB at 13 GHz, increasing 1.4 dB at 18 GHz. The remaining coupling losses for both couplers were less than a few tenths of a dB. A photograph of the two-coupler assembly is shown in Fig. 8. The insertion loss for each output port of the assembly including the line losses is plotted versus frequency in Fig.



4.8 dB Coupler



3 dB Coupler

Fig. 4—Interdigitated coupler layout.

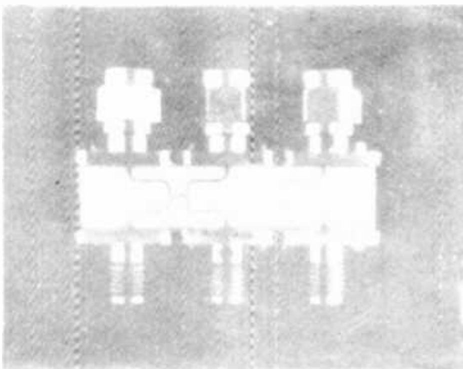
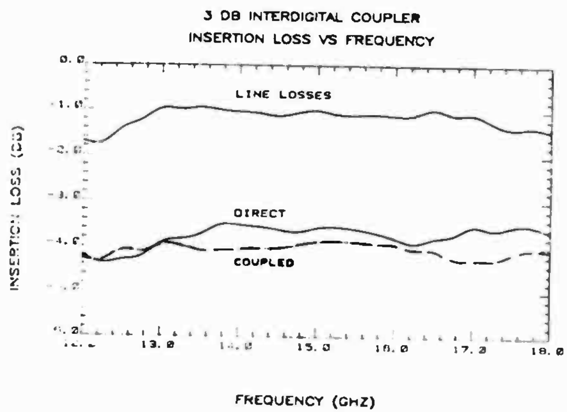
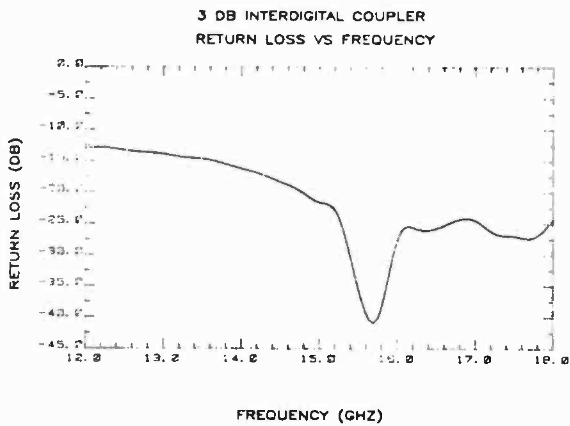


Fig. 5—Coupler characterization circuit.





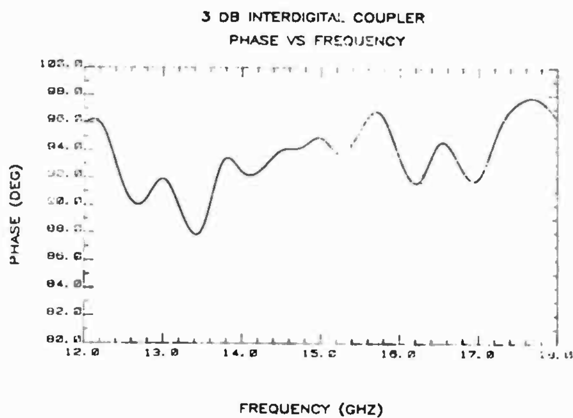


Fig. 6—Performance of 3-dB interdigital coupler.

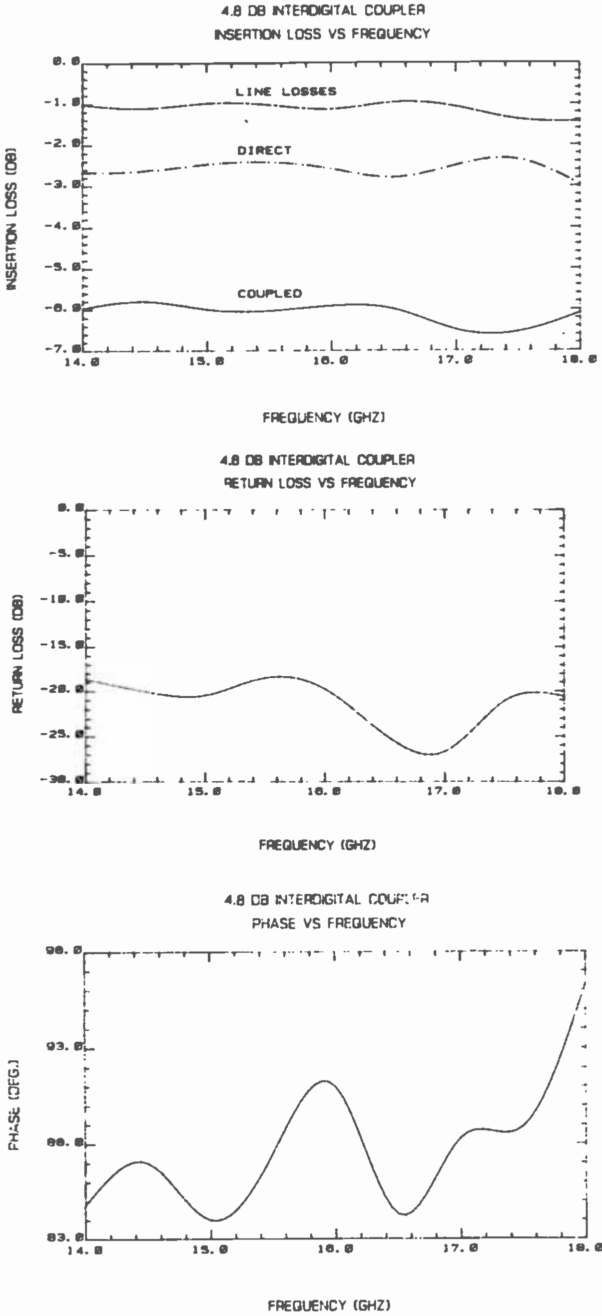


Fig. 7—Performance of 4.8-dB interdigital coupler.

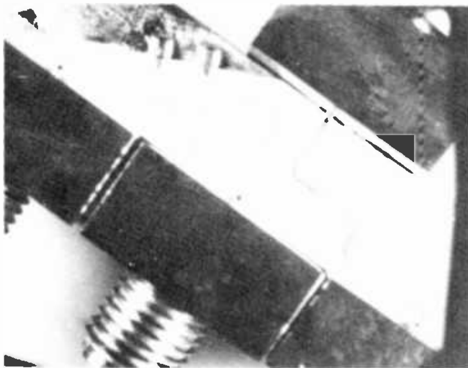


Fig. 8—Two-coupler assembly.

9 and the phase error is shown in Fig. 10. The ordinate in Fig. 10 represents the phase error of vectors one and three with respect to vector two. The designed-in vector separation of 60° has been subtracted from the measured difference to improve the data resolution. The coupler assembly provides a total of only 0.3-dB coupling variation and ±3.5° phase tracking error between all three ports from 16 to 16.5 GHz.

A dual-gate FET amplifier was designed around the nominal S-parameters of the NEC 46300 device.* The grounded source device includes

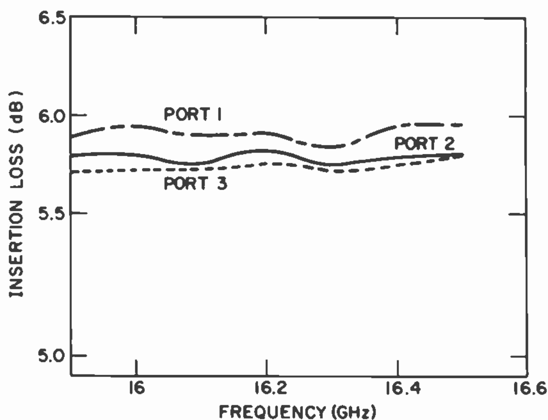


Fig. 9—Coupling of two-coupler assembly.

* Nippon Elect. Co., Ltd.

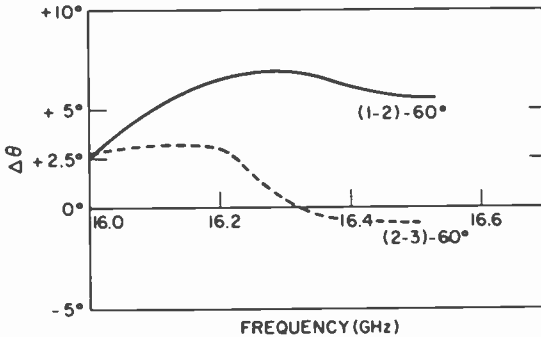


Fig. 10—Phase tracking of two-coupler assembly.

a third port formed by the second-gate-to-source-impedance. This port cannot be easily characterized using the 2-port measurement equipment. The impedance of the second gate G_2 was therefore varied in discrete steps while the standard 2-port S-parameters were measured. The equivalent circuit for the resulting amplifier is shown in Fig. 11. It was necessary to minimize the G_2 series inductance to obtain stable operation with the desired gain in the 16-GHz range. Numerous devices were characterized and a design tolerant to typical parameter spreads was developed (Fig. 12). The circuit is constructed on 15 mil alumina and uses distributed circuit elements. This approach results in very consistent unit-to-unit performance. Typical maximum gains ($V_{G2} = 0$) for six constructed amplifiers are 10 dB with variations of less than ±0.5 dB over the 15.8 to 16.7 GHz band. This performance is obtained without individual circuit tuning. The gain of each amplifier can be adjusted over a range of more than 30 dB by varying V_{G2}, as shown in Fig. 13. The gain and noise figure versus percent of saturated drain current is shown in Fig. 14. The amplifier gives low-noise performance of 5.6 dB with 8.9 dB gain at an I_{DS}/I_{DSS} ratio of 0.18. The current is determined by the bias on gate 1. A typical ouput power at 1-dB gain compression for maximum gain biasing conditions is +7 dBm.

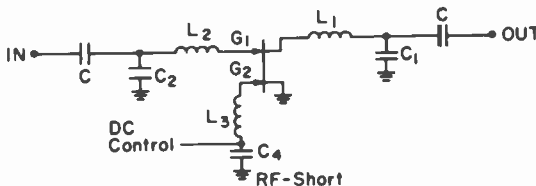


Fig. 11—Dual-gate FET amplifier equivalent circuit.

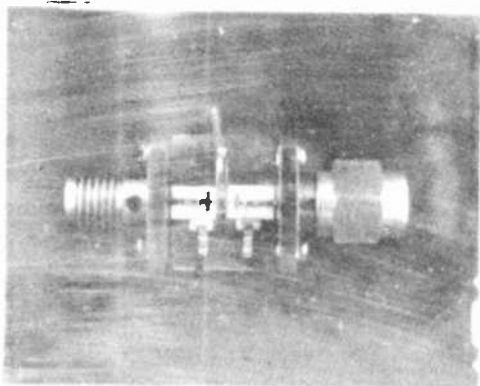


Fig. 12—Dual-gate FET amplifier.

The alternate 3-amplifier configuration shown in Fig. 2 was not used in the module, since it requires the development of a 3-to-1 in-phase combiner as well as the input coupler assembly. This configuration would, however, result in lower coupling losses and an additional significant size reduction if direct combining can be achieved at the drains of the devices. A computer simulation that uses matching of the directly connected device drains was developed. This simulation used the measured S-parameters of the constructed 4.8- and 3-dB couplers, the S-parameters of the actual input matching circuits used for the amplifiers, and the paralleled output S-parameters of the dual gate FETs for different gain settings corresponding to the full 0 to 360° phase shift. A lumped-element output matching circuit was then designed. The results clearly demonstrated the feasibility of this approach. Stable simulated operation was achieved over the full 360° phase shift. Module gains of

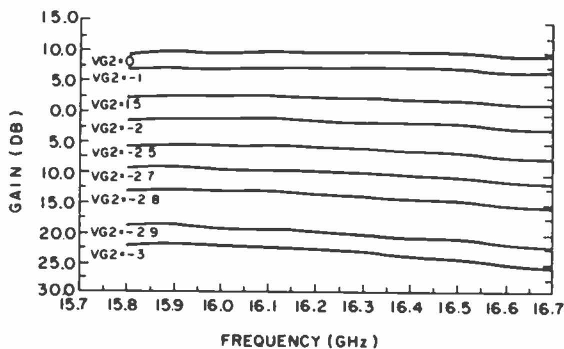


Fig. 13—Dual-gate FET gain control versus frequency.

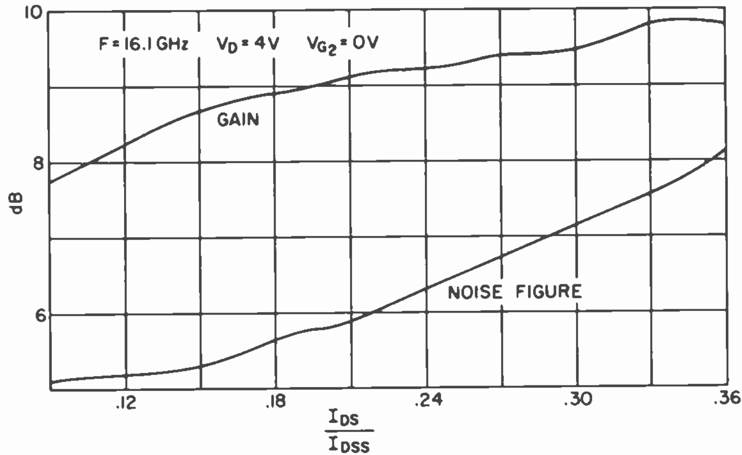


Fig. 14—Gain and noise figure versus normalized drain current.

between 2.1 and 3.2 dB are possible over the 16 to 16.5 GHz range. These gains are larger than can be expected using either the coupler-combiner of the present configuration or an in-phase transmission line combiner. The three-amplifier approach, combined with the lumped-element circuit output matching of the combined devices, can result in a two-order reduction of the module's size.

Experimental Results

The experimental phase/amplitude control module consists of two dual-coupler assemblies and three dual-gate FET amplifiers as shown in Fig. 15. Phase tuning as a function of the amplifier second-gate gain control voltages (V_{G2}) is shown in Fig. 16. Here one gate voltage is kept at 0 V, one at −3 V, while the third one is varied between 0 to −3 V to cover, in each case, approximately 60° phase shift. Under these conditions the amplitude varies by about 7.5 dB over the full tuning range from 0° to 360°.

The theoretical minimum amplitude variation of the resultant vector is 1.3 dB. The additional variation can be attributed to two causes. The first is a dependence of the phase shift through each amplifier as a function of amplifier gain. A typical phase change of 30° occurs over a 25-dB change of gain. Since the phase shift is probably due to the voltage-variable gate-2 capacitance, measurements of phase versus G_1 bias with constant G_2 bias were made. The change of phase using the G_1 variable was reduced to 20° for a gain variation of 25 dB. This operating mode has, however, the disadvantage of large drain current variations

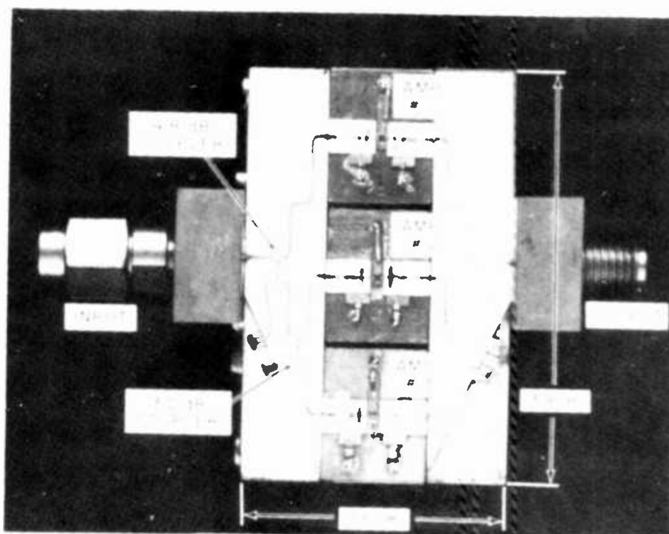


Fig. 15—Phase/amplitude control module.

that accompany the gain changes. The second and less significant cause for the amplitude-versus-phase variations is the imperfect matching between the amplifiers' output and coupler input ports. Further circuit optimization would eliminate this problem.

A constant amplitude output can be achieved over the full 360° phase shift by using the appropriate gate-voltage control functions. Figs. 17 and 18 show the respective functions used for a constant gain of −6 and −28 dB at a fixed frequency of 16.3 GHz. It is only necessary to vary two of the three gate voltages to cover a 120° phase segment with any desired gain. A phase/gain control circuit can therefore be implemented using only two D/A converters and switching circuitry.

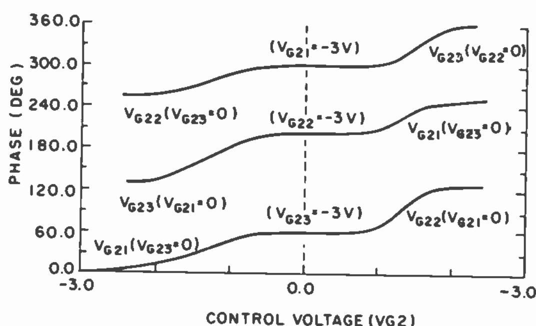


Fig. 16—Phase versus control voltage of the phase shifter.

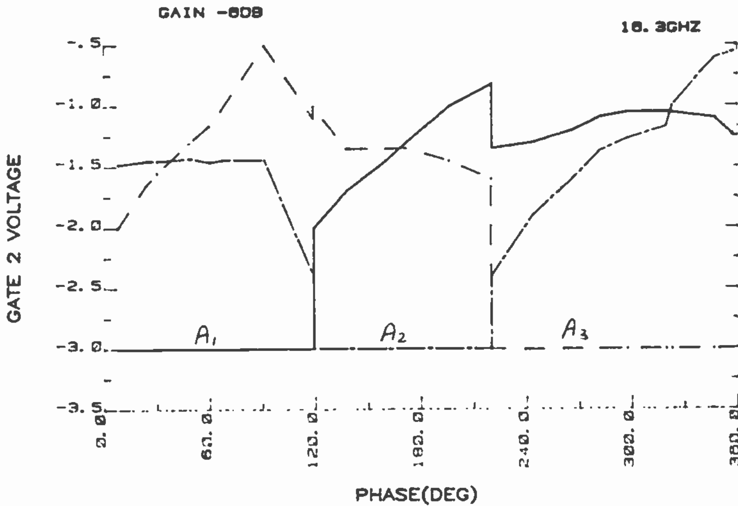


Fig. 17—Control function for constant gain (−6 dB) versus phase.

Both the phase shift and output amplitude can be controlled to any desired accuracy if the operating frequency is known. This is the case for transmitters or fixed-frequency receivers. For applications using wideband receivers operating with variable and unknown frequencies, the instantaneous bandwidth becomes an important operating param-

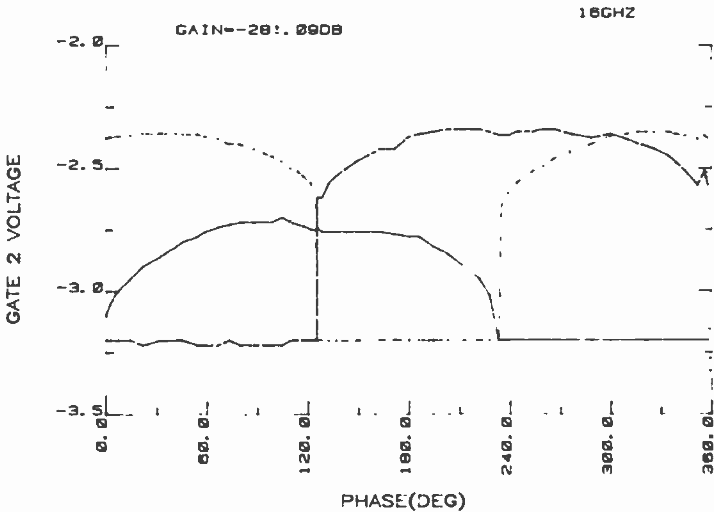


Fig. 18—Control function for constant gain (−28 dB) versus phase.

eter. The instantaneous bandwidth in this case is defined as the bandwidth for fixed control functions over which the phase or amplitude varies from nominal by less than a stated amount. A fixed gate-control function that provides constant gain versus phase at one frequency will result in deviations at other frequencies from the desired gain and phase. The theoretical 1-dB instantaneous bandwidth for this module assuming three perfectly matched amplifiers having constant phase-versus-gain characteristics is approximately 2 GHz. In actuality, dual-gate FET device characteristics vary from unit to unit causing each amplifier's phase and gain characteristics to be somewhat unique. Port-to-port phase-tracking-versus-frequency errors also occur within the coupler assembly.

The amplitude and phase variations for the control module are shown in Figs. 19 and 20. These curves are referenced to control functions that are established for a constant gain of −6 dB at 16.3 GHz. The measured 1-dB and 3-dB bandwidths are 125 and 450 MHz, respectively. The abscissa denotes the values at 16.3 GHz while the ordinate reflects the change that occurs over frequency. Note here that the amplifier that operates in the 0° to 120° and 240° to 360° ranges contributes significantly to the phase errors, while the other two amplifiers contribute less, as shown in the 120° to 240° range. The phase tracking is maintained within 7° over a 200 MHz band. No attempt was made to compensate the module for either the phase or amplitude temperature dependence.

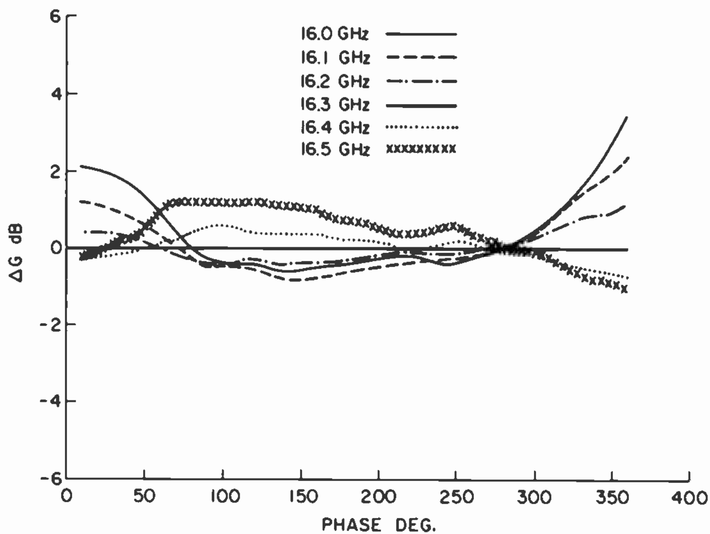


Fig. 19—Gain error versus phase.

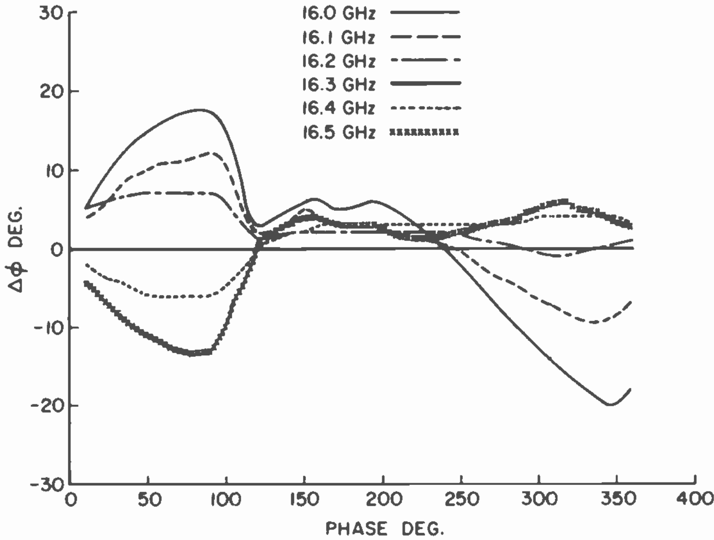


Fig. 20—Phase error versus phase.

Temperature compensation could be achieved by including both temperature-sensitive gate biasing circuits and temperature-sensitive capacitors that are designed into the rf matching circuitry. The module noise figure measured at 16.1 GHz is plotted versus gain in Fig. 21. The noise data is essentially unchanged versus phase.

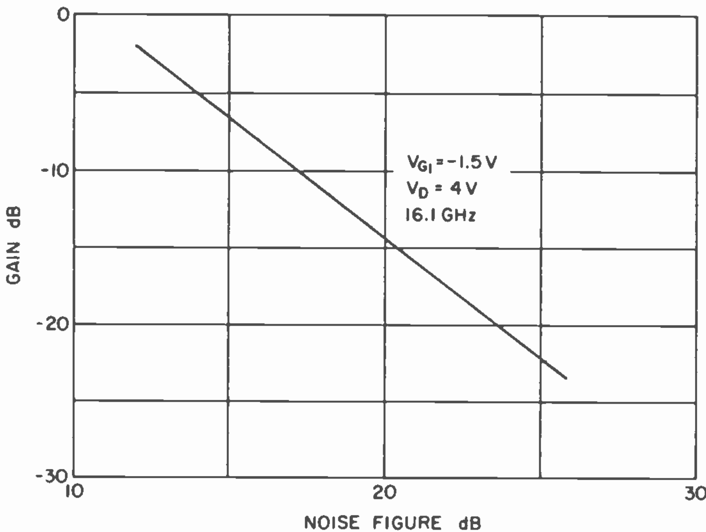


Fig. 21—Phase shifter gain versus noise figure.

Conclusion

A continuous phase/amplitude control module using three rf devices was developed. The Ku-band module has a 0 to 360° phase shift capability with a simultaneous amplitude control range of from −6 to −28 dB. The gain of three dual-gate FET amplifiers as determined by voltages applied to their respective second-gates sets the resultant amplitude and phase shift of the output. These voltages can be quickly and accurately set using two D/A converters and a switching arrangement.

A disadvantage of the three-vector phase shifter is the bandwidth limitation due to the 30° line lengths used in the coupler assemblies. However the three-vector module has a lower parts count, requires less addressing, and is potentially smaller and lighter than the four-vector configuration. This approach when realized in a hybrid integrated circuit with direct device drain combining results in an extremely compact phase/amplitude control module, with very low parts count, suitable for a variety of adaptive phased-array applications.

Acknowledgments

The authors wish to thank Dr. Erwin Belohoubek for his many contributions to this work including the three amplifier phase shifter approach, Richard Brown and Kathleen Lev for their circuit processing expertise, and Edward Mykietyn and Paul Czajkowski for their skilled circuit assembly.

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Silicon as a Millimeter-Wave Monolithically Integrated Substrate—A New Look*

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Abstract—Materials suitable for use as monolithic substrates are summarized. A study of the properties of silicon substrates as transmission line media shows that serious consideration should be given to them for use at mm-wave frequencies. It is concluded that for silicon resistivities of 2000 ohm-cm or greater, microstrip loss in silicon at mm-wave frequencies is only slightly higher than that in GaAs or alumina. The cross section width of a transmission line represents an appreciable part of a wavelength when microstrip is used as an impedance transformer at mm-wave frequencies. Therefore, substrate thickness (using the latest dispersion characteristics) is especially considered in circuit design. These effects on the design of 3-dB interdigitated and branch-line couplers are demonstrated.

Fabrication of silicon IMPATT diodes operating up to 200 GHz has been accomplished by novel techniques that maintain the silicon's high resistivity. We report on diodes yielding 25 mW cw at 102 GHz, 16 mW cw at 132 GHz, and 1 mW at 195 GHz. The techniques described are ion implantation, laser annealing, unique secondary-ion mass spectrometry (SIMS) profile diagnostics, and novel wafer thinning. The utilization of these technologies paves the way for the processing of silicon monolithic mm-wave integrated circuits.

1. Introduction

One of the major goals of microwave research in the past several years

* This paper is based in part on excerpts from our papers in the IEEE Trans. MTT[3] 1982 and in the SPIE Proceedings of the Conference on Integrated Optics and Millimeter and Microwave Integrated Circuits Vol. 317, 1982.[4]

has been the development of the technologies needed to fabricate monolithic microwave (mm-wave) integrated circuits. This goal has now been attained. Since the introduction of the microstrip for use in microwave integrated circuits[1] in 1965, the pros and cons of hybrid versus monolithic circuits have been debated. Although still an item of contention, the role of hybrid technology below 36 GHz seems to be assured in present planning. However, the potential advantages of monolithic circuits above 40 GHz make their use at even higher frequencies the most favored approach for future applications.[2] Parasitic inductance, normally encountered in forming devices and circuits, is reduced and controlled in the monolithic approach, making it a most attractive technique for use in millimeter-wave circuits. The silicon IMPATT diodes are the only solid-state microwave devices presently capable of delivering the required power output of hundreds of mill-watts at 100 GHz. High-resistivity bulk silicon is an adequate substrate for use in EHF monolithic integrated circuits, provided modern silicon processing technologies such as ion implantation, laser annealing, and wafer thinning are utilized to fabricate the ICs. For example, the processing temperature must not exceed 800°C if the required high resistivity of the bulk silicon starting material is to be preserved. We will consider:

(1) the pros and cons of materials considered for use as monolithic substrates at mm-wave frequencies;
(2) the properties of microstrip, with attention to both dielectric and conductor losses;
(3) the effect of shorter wavelengths (with increasing frequency) as the wavelengths become comparable with microstrip cross section;
(4) a novel technology for the fabrication of mm-wave devices utilizing ion-implantation, laser annealing, and unique SIMS diagnostics.

2. Materials for Monolithic Approaches

Our discussion of the possible materials for monolithic approach in EHF is based on the premise that the circuit will be processed around available devices. The silicon IMPATT currently dominates as a power device at EHF; therefore, silicon monolithic transmitters should be seriously considered.

The following are the advantages and the disadvantages of various substrate materials, for the monolithic approach.

Silicon-on-Sapphire

Sapphire is one of the best insulators for use as a transmission substrate, and the suggestion to grow silicon on it for monolithic microwave circuits dates back to 1966.[6,7]

(a) Advantages
Silicon is used only where devices are included, while the sapphire, a superior insulating substrate, is present as the passive substrate.
(b) Disadvantages
Difficult to contact ground plane; via holes are required.
Silicon grown on sapphire to date has not proven suitable for high-frequency devices.

This technique is not sufficiently advanced for consideration at this time.

Gallium Arsenide

Gallium Arsenide is the material presently under consideration for lower-frequency monolithically integrated circuits. Its use at frequencies below 35 GHz is under development.[8]

(a) Advantages
Above 40 GHz: Schottky-barrier mixers, IMPATTs, and Gunn devices have been made.
Below 45 GHz, FETs up to K-band have been developed.
Good insulator material (up to 10^8 Ω-cm).
(b) Disadvantages
Its use has not yet become an established technology, compared to that of silicon.
Above 40 GHz, power devices are not thus far within the state-of-the-art.
Large wafers are not yet readily available.
Heat conduction is one-half that of silicon.

Gallium arsenide substrates are not yet suitable for use in high-power mm-wave transmitter modules, but they may be ideal for i-f and receiver modules. It is worthwhile mentioning that silicon could also be used for the receiver module, excluding the local oscillator which. at this point, has to be a Gunn device.

Silicon

The use of high-resistivity silicon as a substrate for microwave circuits was first seriously investigated in 1965. Circuit losses introduced by the dielectric were found to be minimized by a high-resistivity substrate. Measurements on 1400-Ω-cm silicon at 10 GHz have yielded respectable losses for microstrip circuits.[5] Silicon substrates of 2000 to 10,000 Ω-cm are presently available, the use of which further minimizes substrate loss. However, because the high temperatures required in device processing destroys its intrinsic properties, the use of silicon as a substrate was

abandoned. Today, it *is possible* to use ion implantation and selective laser annealing to create devices without increasing substrate temperature, and the high-resistivity silicon can, therefore, be used as a substrate material for millimeter-wave circuits. Since silicon of high resistivity can be obtained and maintained, a new range of possibilities is open to use, particularly for mm-waves. The advantages and disadvantages of using silicon as a basic material for monolithic circuits are listed below.

(a) Advantages
Silicon use is based on a well-established technology.
Above 35 GHz, high-power IMPATTs, PIN diodes, varactors, and devices for transmitting circuits are within the state-of-the-art.

(b) Disadvantages
Intrinsic insulating qualities are degraded by temperatures above 800°C.
Bipolar devices are not achievable above X-band.
Gunn devices are not feasible.

We conclude that through the use of modern processing technology, silicon once again offers exciting possibilities, particularly for monolithic millimeter-wave transmitters and amplifiers.

The use of silicon is particularly attractive because we have successfully fabricated high-frequency silicon IMPATT devices using selective ion implantation and laser annealing, and we have obtained state-of-the-art devices without necessarily raising the temperature of the whole substrate. Intrinsic silicon can now be used, and the high resistivity can be maintained throughout the device fabrication steps. Thus, the main objections to the use of silicon have been removed. We have examined the properties of silicon and the transmission lines obtained using intrinsic Si as a substrate for microstrip from 40 to 100 GHz. In a way, a new world for monolithic mm-wave circuits has been reopened.

3. Microstrip Lines on Intrinsic Silicon

A technique explored in the early days of MIC technology was that of microstrip lines on silicon. In 1965, T. M. Hyltin[5] demonstrated reasonable losses at 10 GHz using silicon of 1400-Ωcm resistivity.

Microstrip on silicon has been examined in many laboratories. At RCA in 1973, Sobol and Caulton[2] presented an analysis of silicon microstrip properties including conductor and substrate losses. Gopinath[9] analyzed microstrip, including radiation losses when GaAs substrates were used. Typical results are displayed to demonstrate silicon microstrip properties. Fig. 1 (Fig. 9 of Ref. [2], modified) demonstrates the relative

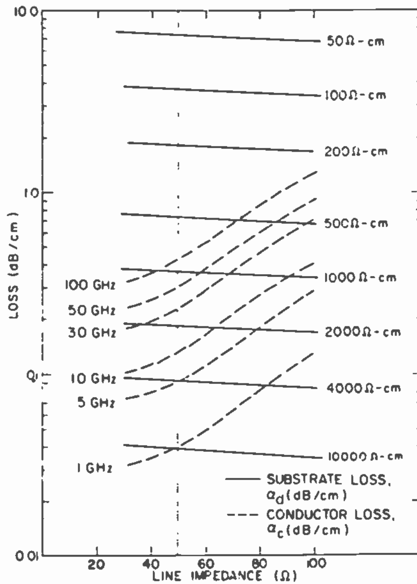

Fig. 1—Conductor and substrate losses (in dB/cm) of microstrip lines on Si substrates.

contributions of substrate and conductor losses versus characteristic impedance. We conclude that (1) at the higher frequencies (>30 GHz), the conductive loss dominates, (2) the substrate loss is independent of frequency, and (3) if the resistivity of the substrate is 2000 Ωcm or greater, it will not contribute significantly to the total loss. Fig. 2 (Fig. 11 of Ref. [2]) shows the sum of the conductive and Si substrate losses versus frequency for 50-Ω lines on 10-mil-thick Si and GaAs substrates. A comparison between theoretical and measured losses[5] on a silicon substrate microstrip is shown in Fig. 3. The agreement is excellent. Fig. 4 (Fig. 2 of Ref. [4]) demonstrates the measured total loss (up to 18 GHz) of a 50-ohm line on an 8-mil-thick (5000 ohm-cm) silicon substrate, indicating a variation of 65% from the calculated values shown in Fig. 2.

We use the equations presented by Schneider[10] to compare the loss factor α of our Figs. 1 and 2 with the Q of a resonator:

$$Q = \frac{20\pi}{\ln 10} \frac{1}{\alpha\lambda}$$

where λ is the guide wavelength. Pertinent data are

Fig. 1 (10-mil Si): 50 GHz, α_c = 0.3 dB/cm, λ = 0.23 cm[11], $\alpha\lambda$ = 0.069 dB, Q = 395;

Fig. 2 (10-mil Si): 50 GHz, α = 0.33 dB/cm, λ = 0.23 cm, $\alpha\lambda$ = 0.076 dB, Q = 359;

Fig. 5 (4-mil Si): 60 GHz, α = 1.78 dB/cm, λ = 0.19 cm, $\alpha\lambda$ = 0.34 dB, Q = 80.

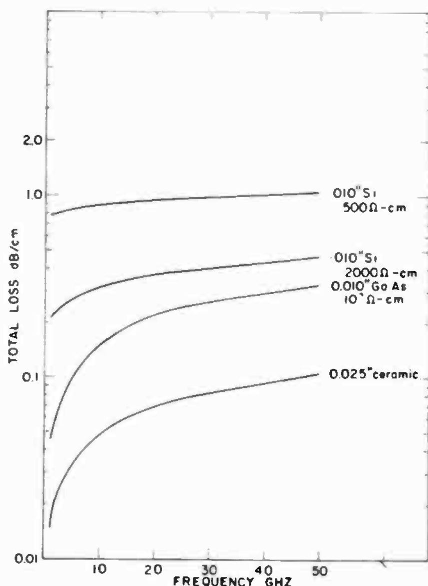

Fig. 2—Loss (in dB/cm) as a function of frequency for 50-ohm microstrip lines on Si, GaAs, and ceramic substrates. Loss includes both α_c and α_d.

The dielectric Q_d is related to the resistivity ρ by[12]

$$Q_d \sim \omega\rho\epsilon \approx \omega/\omega_d,$$

where ϵ is the dielectric permittivity for silicon ($\epsilon = 11.8 \times 8.85 \times 10^{-14}$ farads/cm). ω_d may be defined as a dielectric relaxation frequency,

$$\omega_d = \frac{1}{\rho\epsilon}.$$

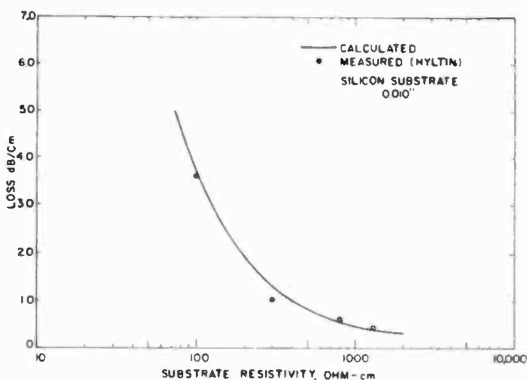

Fig. 3—Loss (in dB/cm) as a function of substrate resistivity for 50-ohm microstrip line on Si substrate (measurements and calculations for 10 GHz). From Ref. [5].

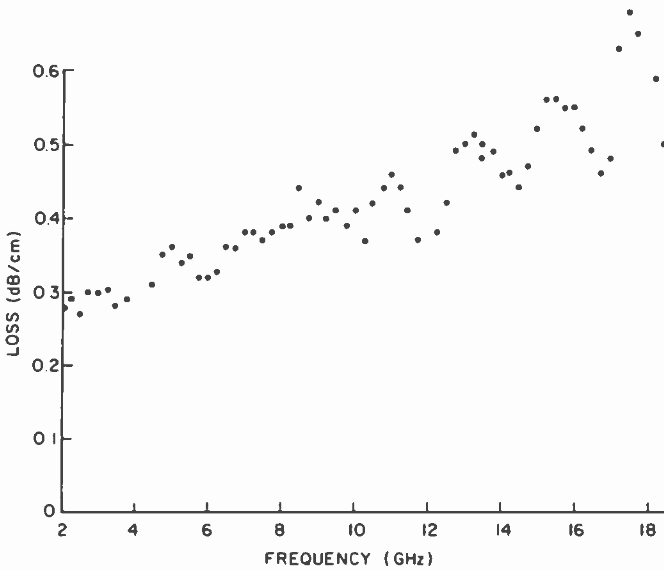

Fig. 4—Measured loss versus frequency of 50-ohm microstrip line. Substrate 5000 ohm-cm silicon, 8-mil thick, Au line 6.4-mil wide.

Above the frequency ω_d, the substrate appears primarily as a resistive material. Fig. 6 shows $f_d = \omega_d/2\pi$ for GaAs and Si, as a function of temperature. The figure displays an estimate of a lower limit on the operating frequency. We are using Fig. 6 to compare the measured change in loss as a function of temperature via the previous equations

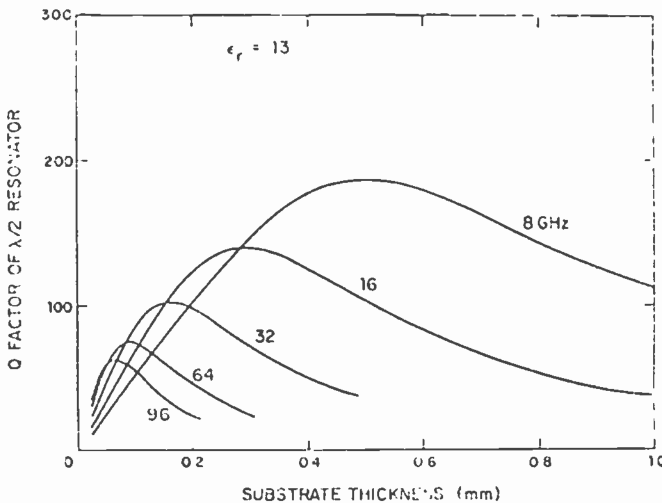

Fig. 5—*Q* factor versus substrate thickness for 50-Ω transmission lines. Reprinted from Gopinath[9] (Fig. 3e of Ref. [9], IEEE 1981).

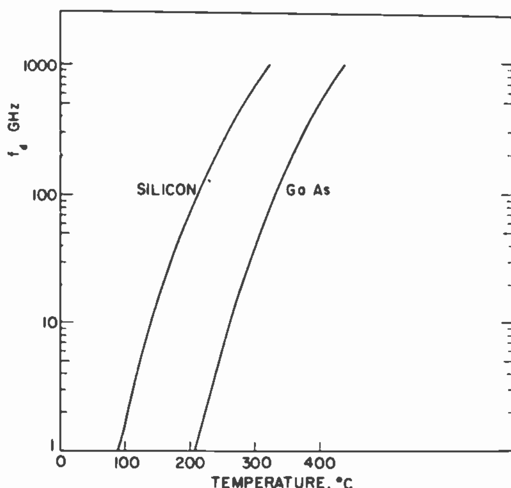

Fig. 6—Dielectric relaxation frequency of Si and GaAs substrates as a function of temperature.

of Q_d and ω_d. For example, at 60 GHz, for ρ = 10,000 Ω-cm, Q_d = 3937 and for ρ = 2,000 Ω-cm, Q_d = 787.

The relationship between Q and the dielectric loss tanδ takes into account the effective dielectric constant $\epsilon_{r_{eff}}$[13]:

$$\frac{1}{Q_d} = \frac{\dfrac{1}{\epsilon_{r_{eff}}} - 1}{\dfrac{1}{\epsilon_r} - 1} \tan \delta.$$

This relationship occurs because ϵ_r does not completely fill the media. $\epsilon_{r_{eff}}$ = 6.755 and for Q_d = 3937,

$$\tan\delta = 2.7 \times 10^{-4}$$

while for Q_d = 787,

$$\tan\delta = 1.35 \times 10^{-3}.$$

The attenuation is related to the substrate parameters by

$$\alpha_d = \frac{20\pi}{\ln 10} \frac{1}{Q_d \lambda}$$

$$\alpha_d = \frac{10}{\ln 10} \frac{\sqrt{\epsilon_{r_{eff}}}}{\rho e \, (3 \times 10^{10})} \text{ dB/cm}.$$

α_d is thus almost independent of frequency, although tanδ and Q_d are not. For example, for ρ = 2000 Ω-cm, α_d = 0.18 dB/cm, as shown in Fig. 1. Note that in Fig. 2, the total loss of 50 GHz only increases from 0.33

dB/cm to 0.47 dB/cm with a decrease of dielectric resistivity from 10^7 to 2×10^3 Ω-cm.

Fig. 5 is a plot of Q for various frequencies (including radiation) versus substrate thickness for GaAs, the loss of which is close to that of silicon at high frequencies (taken from Ref. [7], Fig. 3e). For operation at 60 GHz, a thickness of 0.1 mm, or 4 mils, will allow the achievement of a Q of 80, corresponding to an α of 0.62 dB/cm, as shown previously. This necessitates the use of a 3-mil-wide metal for a 50-Ω line, a disadvantage for reproducibility and accuracy. When the circuit is shielded in a waveguide below cutoff, radiation poses no problem and 10-mil or thicker substrates can be used. Fig. 2 would then apply.

The figures presented here allow us to draw some conclusions. At low frequencies, silicon microstrip for microwave integrated circuits incurs great losses compared to alumina and GaAs. Fig. 1 shows that for frequencies below 30 GHz, the substrate loss of silicon (2000 Ω-cm) is equal to or greater than the conductor losses; for GaAs, which has a resistivity of greater than 10,000 Ω-cm, the conductor loss at 1 GHz is far greater than the substrate loss. Fig. 2 shows that the total losses of silicon and GaAs microstrip are comparable above 40 GHz. Two thousand ohm-cm (or greater) silicon is a viable substrate for frequencies above 30 GHz, where conductor and radiation losses dominate. The above conclusion assumes that the high-resistivity property can be maintained throughout all the processing steps. At RCA Laboratories, we have successfully processed and fabricated diodes using very thin wafers, as will be described. This process involves ion-implantation and laser-annealing, techniques that do not alter substrate resistivity.

A silicon dielectric, or image line,[14] has very low loss at high frequencies. Therefore, it is suitable for frequencies above 100 GHz. Techniques to integrate this image line with microstrip devices can lead to feasible monolithic components.

Our experience has shown that at frequencies greater than 30 GHz, the use of silicon microstrip is acceptable provided resistivities of 2000 Ω-cm and higher can be maintained. Modern technology makes it possible to fabricate devices without deterioration of the material resistivity, which was impossible in 1965 when silicon monolithic circuits were first proposed for microwaves. The use of silicon microstrip is now feasible, therefore, from 30 GHz and above with reasonable loss, and dielectric and image lines are available to extend the frequency range beyond 100 GHz. Measurements of microstrip losses at 60 GHz are of critical importance. It is well known that the microstrip is a relatively high-loss transmission line when compared with waveguides, especially on a per-unit-length basis. At high frequencies, however, the loss per wavelength is small due to the physical length.

4. Microstrip Circuits at High Frequency

Transmission lines at high frequencies exhibit a new problem. As the frequency increases, the wavelength shortens. The cross-sectional width W (nearly constant or increasing because of dispersion) thus becomes an important fraction of a wavelength, with resultant phase changes across the transverse dimension. Some of the first circuits built under this constraint are 3-dB couplers that we are studying for use as a key element for a two-stage amplifier in silicon.

An initial coupler being considered is the Lange coupler (interdigital). This is the widest bandwidth microstrip approach amenable for batch fabrication. The circuit design and configuration of a Lange coupler are shown in Fig. 7. The design of the interdigitated coupler has been successfully demonstrated at Ka-band and can be scaled to a chosen frequency. The length of the hybrid is $\lambda/4$. The width of the line and spacing between the lines, W and S, respectively, are determined for given substrate thicknesses using the Bryant and Weiss tables and standard techniques. At the RCA Microwave Technology Center, we have developed a computer optimization routine that is very useful in predicting the performance of the hybrid. For a four-line interdigitated hybrid on a 200-μm-thick Si substrate ($\epsilon_r = 11.8$), the following results are obtained:

$$W/H = 0.065;\ W = 13\ \mu\text{m and } H = 200\ \mu\text{m};$$

$$S/H = 0.07;\ S = 14\ \mu\text{m and } H = 200\ \mu\text{m; for } \lambda/4 \text{ at } 45\text{ GHz}.$$

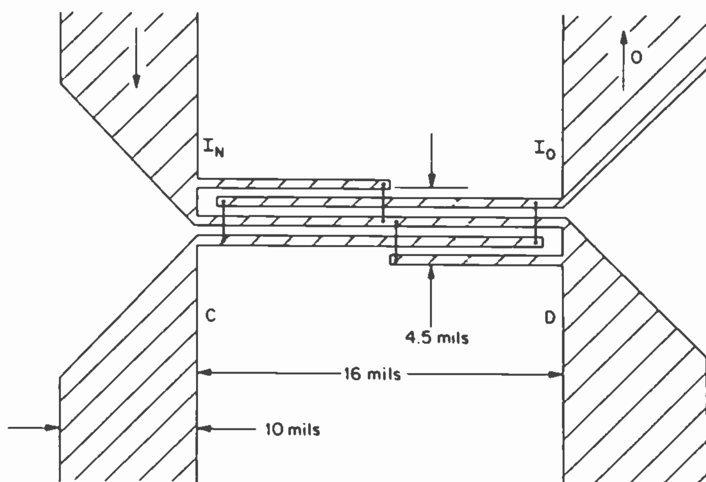

Fig. 7—A Lange coupler for 60-GHz applications.

Fig. 7 represents the coupler design for use on silicon substrate at 60 GHz. The important problems illustrated (the coupler is drawn to scale) are as follows. (1) Although the bonded points are to be at the same potential, the cross section is large compared to a quarter wavelength. The coupler's performance is uncertain at this time, because of the standing-wave pattern in the cross-sectional area. (2) The size of the lines (0.5 mils width and separation) makes the coupler difficult to fabricate.

Another coupler being considered is the quadrature branch-line coupler. It consists of two 50-ohm and two 35.3-ohm lines, each $\lambda/4$ long. For this coupler to operate at high frequencies, the $\lambda/4$ cross-sectional width should be large, and rectangular breaks are to be avoided. Fig. 8 illustrates the respective dimensions of a microstrip line and Fig. 9 shows a possibly-acceptable design on 6-mil silicon, drawn to scale. Results of this coupler on 8-mil alumina at 50 GHz have been reported.[15]

Yamashita, et al,[16] have proposed the latest high-frequency microstrip dispersion curves based on theory as well as experiment. These curves have been incorporated into a computer program, whereby we calculate impedance and width as a function of ϵ_r (dielectric constant) and of substrate height H. Table 1 lists characteristics for $\lambda/4$, cross-section W, and a figure of merit L/W, for various substrates and thicknesses with the objective of verifying if 3-dB couplers can be fabricated. The higher the figure of merit, the longer the microstrip line, L, compared to the cross sectional width, W (Fig. 8). Fig. 10 is the scale drawing of a 60-GHz coupler on 10-mil silicon. The figure of merit, 1.6, is not promising and as seen, the lines merge into one another. However, the coupler on 6-mil Si (Fig. 9) has a figure merit of 3.1.

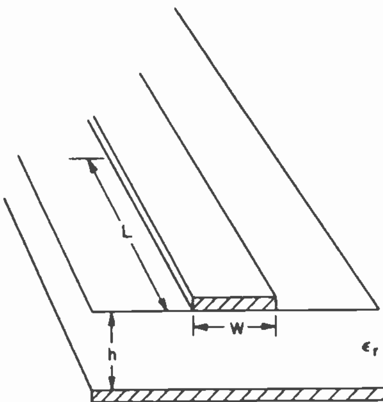

Fig. 8—Dimensions of a microstrip line.

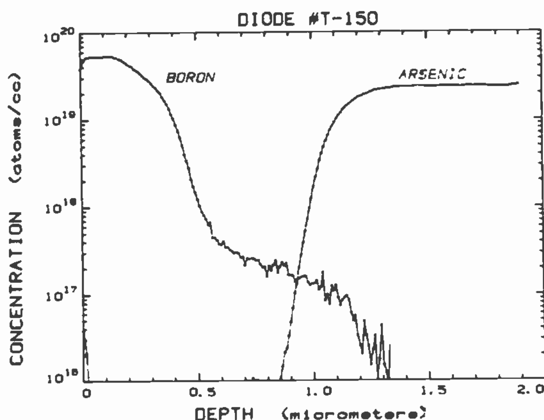

Fig. 12—SIMS depth profiles of epi-grown p and ion-implanted p^+ on n^+ arsenic-doped substrate.

silane (SiH_4) decomposition method. All the silicon layers are deposited at a substrate temperature ranging from 1000°C to 1050°C. Diborane or arsine gas is introduced during the epitaxial growth process to achieve the desired impurity concentration in the respective layers.

B. Growth

The substrates' back surface and side edges were coated with 2000 Å of deposited oxide. The substrates were heated to approximately 1150° and etched with HCl (1% HCl for 5 minutes). The temperature was then dropped to approximately 1050°C and the first epi-layer was grown. The system was then purged for all reaction gases (at 1050°C) before the second epi-film was grown. The adjustment of crystal growth parameters, using impurity concentration profiles by SIMS, have led to sharp transitions (Fig. 13). The concentration varies from 3×10^{19} atoms per cc in the substrate to 2×10^{17} atoms per cc in the epitaxial layer over a distance of only 3000 Å.

6. Device Fabrication by Ion Implantation and Laser Annealing

6.1 Single Drift Structure

As discussed above, the conventional fabrication technique is via epitaxy. The n layer, followed by p and p^+ layers, are grown in succession upon an n^+ substrate which serves as a handle during the fabrication (this substrate is partially etched away just before the final Cr-Au metallization). When the design frequency of the IMPATT exceeds 140 GHz, the doping profile requirements (e.g., junction abruptness and uniform layer thickness) are difficult to meet using this epitaxial technique.

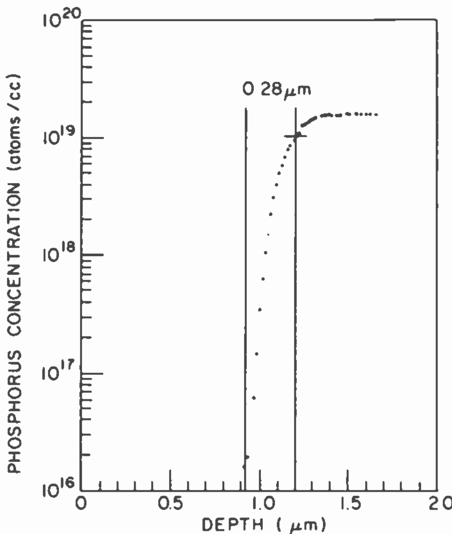

Fig. 13—Impurity concentration profile in transition region.

A novel application has been proposed[22] that uses both ion-implantation and laser annealing techniques to achieve uniformity and reproducibility of the closely-spaced junctions. The single-drift IMPATT was successfully processed as a vehicle for the more difficult double-drift structure. First, an n-layer with doping concentration of about 5×10^{16} cm^{-3} is grown at 1050°C on a (111) oriented n^+ silicon substrate using conventional silane pyrolysis. The thickness of this n-epi layer is 2 μm. Next, two ion implants are carried out under the following conditions:

(1) n region: ^{31}P implant at 500 keV with a fluence of 1×10^{13} cm^{-2}
(2) p^+ region: ^{11}B implant at 50 keV with a fluence of 2×10^{15} cm^{-2}

Typical SIMS analyses of these implants before and after annealing are shown in Figs. 14(a) and (b), respectively. After the above ion-implants, the wafer can be either thermally annealed at 1000°C for 15 minutes in dry N_2 (after depositing 0.5 μm SiO_2 as capping) or laser annealed.

The wafer is then metallized on the p^+ side with Cr-Au and electroplated with 25-μm-thick copper to form the heat sink. Another layer of gold, 2-μm thick, can be plated upon the copper heat sink. This metallization also serves as a handle for subsequent processing. At this point, the n^+ silicon substrate can be completely or partially removed by the procedure for wafer thinning, described in the next section.

Next, the n^+ layer is formed by a 950 keV $^{31}P^+$ ion implant with a fluence of 3×10^{15} cm^{-2}. This implanted layer 0.95 μm in depth is then laser annealed. The laser annealing heats the material to a depth of only

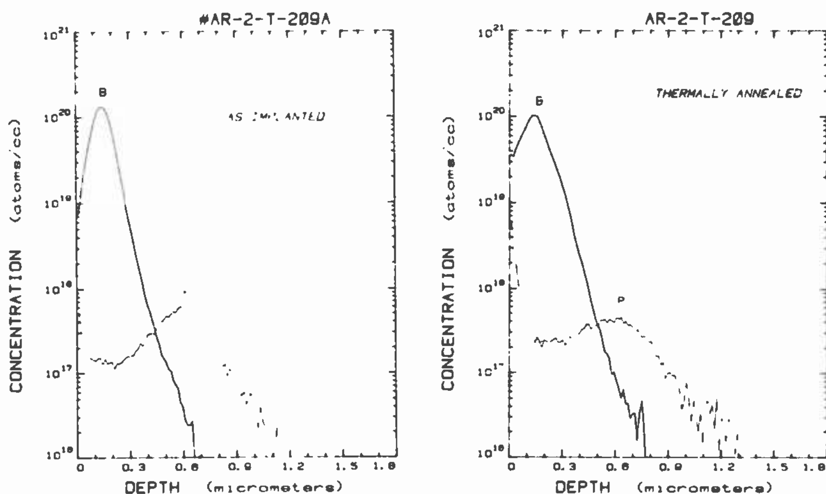

Fig. 14—Results (measured by SIMS) obtained on implanting ^{31}P and ^{11}B in silicon before and after annealing.

one micron and for a very short time (~1 μsec). Thus, there is no deleterious effect at the metal-silicon interface (2 μm away), and profile redistribution is minimized. Laser annealing is necessary here because, at this point in the processing sequence, the above device structure (with one side metallized) cannot be thermally annealed.

The n^+ contact layer is first evaporated with Cr-Au. Then, an array of gold dots is electroplated through a photoresist mask. The unplated metallization is removed, and mesa diodes are formed by etching completely through the unplated area of the semiconductor layer. Finally, the diodes are separated, and each diode, with its attached copper heat sink, is tested. I-V characteristics are shown in Fig. 15. Figs. 16(a), (b), and (c) demonstrate the possibility of processing devices, when even higher penetration is needed, by using higher energy levels.

6.2 Double-Drift Structures

For application of the double-drift diode at around 140 GHz, a mm-wave IMPATT diode with symmetrical structure and total active layer thickness of 0.5 μm is desired. Such a device requires four implants instead of only three. The proposed device is to have a total thickness of 1.5 μm. Hence, an n-epi layer of 1.5 μm thickness and doping concentration of 1×10^{16} cm^{-3} is first grown on an (111)-oriented n^+ silicon substrate. The doping concentration of the n-epi layer is not critical in this case and can be varied within a factor of 2 or 3 without seriously affecting the performance of the finished device. However, the thickness

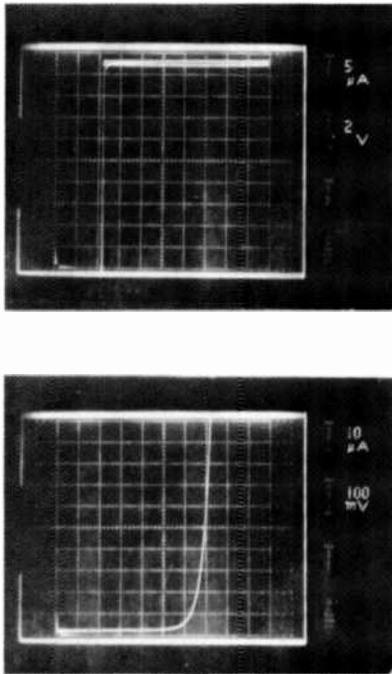

Fig. 15—I-V characteristics of a millimeter-wave IMPATT diode.

of the n-epi should be carefully measured and controlled. The processing is essentially similar to that described in the previous section, except for the insertion of the 0.25 μm n-layer by a $^{31}P^{++}$ ion implantation at 280 keV after the implant for the n^+ contact. The $^{31}P^{++}$ ion implant at 280 keV has the same penetration as a $^{31}P^{+}$ ion implant at 560 keV, which is needed for the deep penetration. Both the n^+ and the n region are laser annealed (simultaneously) as described in the next section.

7. Technology Specifics

7.1 Laser Annealing

Laser annealing was performed with a pulsed Nd:YAG laser.[23,40] The laser beam has a pulse width of 15 nanoseconds and contains both the 1.06 μm and the 0.53 μm components. This is achieved by passing the fundamental output of the two-stage pulsed Nd:YAG laser through a Type II KD*P crystal frequency doubler, which has a conversion efficiency of 30%. The dual output pulses are collinear and are optically scanned over the target wafer. The 0.53-μm component has a higher absorption coefficient in silicon. Therefore, electrons and holes generated

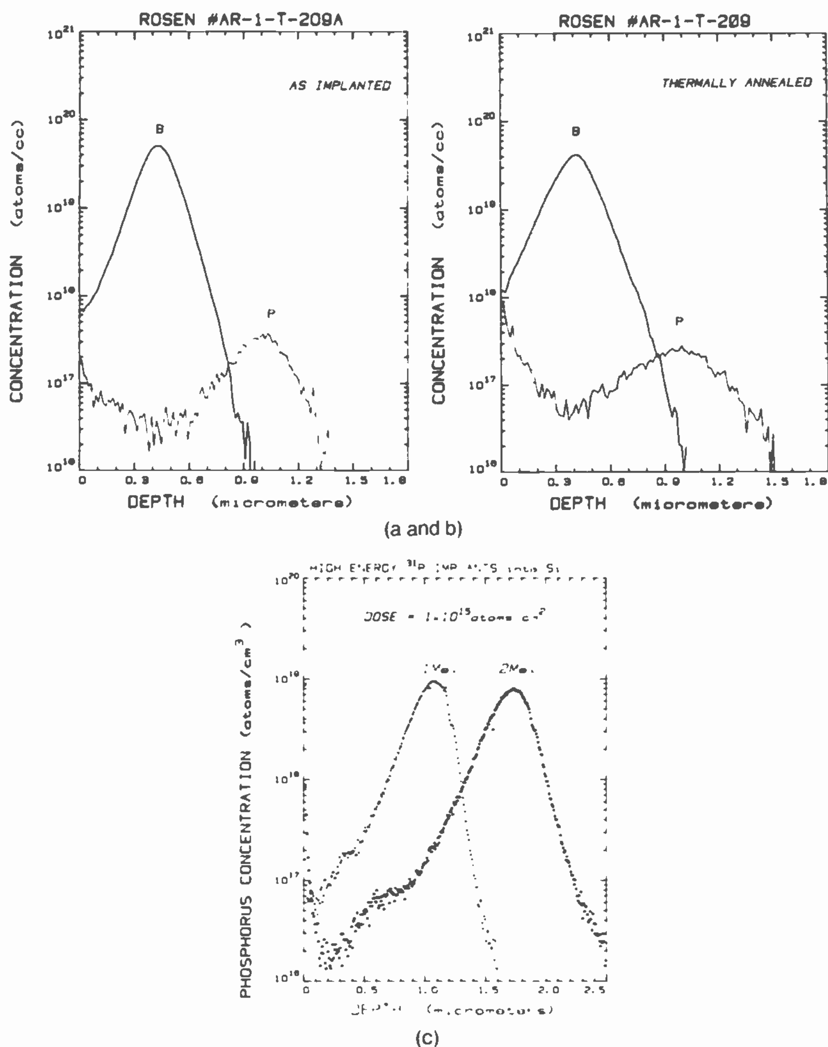

Fig. 16—Results (measured by SIMS) obtained (a and b) on high energy implanting ^{31}P and ^{11}B in silicon before and after annealing and (c) results obtained on ^{31}P implanted into silicon at 1 and 2 MeV.

by the 0.53 μm component enhance the absorption of energy from the 1.06 μm component, which penetrates deeper in silicon and is more suitable for annealing deep implants. The laser beam spot has a diameter of 6 mm, with ~50% overlap between adjacent spots. The pulsed laser is operated at a repetition rate of 10 pulses per second.

Fig. 17 shows the profile distribution determined by SIMS[24-26] of the ion implantation of 50-keV boron into a 10^{16} atoms/cm^3, As-doped,

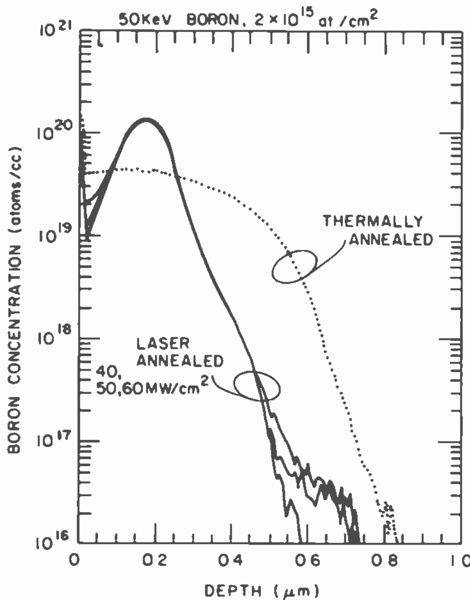

Fig. 17—Profile distribution determined by SIMS comparing effect of laser as opposed to thermal annealing.

epi-grown substrate. The ion-implantation fluence level determines the concentration profiles. The improvement accomplished by the use of laser annealing as opposed to thermal annealing is evident as the sharpness in the profile distribution increases with increasing pulse densities. The ability to obtain the concentration profile by SIMS diagnostics has enabled us to accurately determine the carrier profile resulting from the ion implantation and annealing processes.

7.2 Secondary-Ion Mass Spectrometry

We have built our own instrument[24] for performing secondary-ion mass spectrometry (SIMS). This instrument is particularly well suited for silicon device research because of its Cs^+ primary ion source and its ultra-high vacuum capabilities. We have shown[25] how these attributes have enabled us to profile n-type dopants (P and As) in Si down to concentrations of less than one part per million atomic (ppma). This level of accuracy is normally impossible using a more traditional SIMS instrumentation. Furthermore, we have shown[26] how to depth-profile p- and n-type dopants simultaneously and thus determine electrical junction depths *directly* from the SIMS data. It is this capability that has been of most benefit to millimeter-wave device research. When

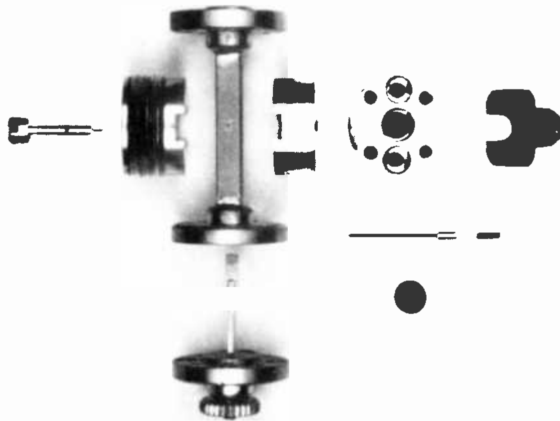

Fig. 18—Disassembled oscillator circuit.

fabricating double-drift diodes by ion implantation, the as-implanted dopant distribution can only be predicted. SIMS is used to measure accurately the p and n dopant distribution after thermal annealing, which is important because diffusion can often alter the profiles in an unpredictable manner, smearing together the very thin layers needed for high GHz operation. We have been successful in determining whether or not the implantation and diffusion steps have produced the desired doping profiles prior to the difficult and tedious steps needed to process the wafers into diodes. SIMS will be of even greater benefit with high-energy (exceeding 1 MeV) ion implantation coupled with laser annealing, because ion ranges at these energy levels are less precisely known and diffusion behavior with laser annealing is, as yet, relatively unpredictable.

7.3 Wafer Thinning

The conventional technique for wafer thinning begins with Cr-Au metallization on the p^+ side to serve as the handle. A hole is opened in the center of the metallization to allow for light transmission measurement to evaluate wafer thickness. The center of the wafer is chemically thinned to as low as 2 μm. The wafer is then supported by the remaining outside ring and the top metallization (with the hole). The thickness of the n-epi

Fig. 19—Reduced-height waveguide circuit.

is then amenable to precision control and measurement.

An extensive investigation of a preferential silicon etch has been launched to enhance our capability to thin substrates uniformly and to selectively remove n^+ material from n.[27]

We have tested an $8CH_3COOH:3HNO_3:1HF$ solution on ⟨111⟩ orientation, n-type wafers. Wafers with impurity concentrations of 10^{13}, 10^{17}, and 10^{19} atoms/cm^3 were used. Several major factors influence the n etch rate: (1) etching two wafers of different impurity levels simultaneously, (2) the presence of gold metallization, and (3) uniformity of the crystal structure. The 10^{19} atoms/cm^3 (n^+) wafers were the least influenced by these factors, since these wafers etched relatively fast (between 2.7 to 3.5 μm per minute). The etch rates of samples with impurity concentration of less than 10^{18} atoms/cm^3 (n) are significantly lower than 3 μm/min. Several examples of these effects are seen in Table 2. An epi

Table 2—Etch Rates

Impurity Concentration (atoms/cm^3)	Etched Alone (μm/min)	With 10^{19} Sample (μm/min)	With Au Metal-lization (μm/min)	With Au Metal-lization and 10^{19} Sample (μm/min)
10^{13}	0.0005–0.0007	0.02	0.04	0.1–0.5
10^{17}	0.003–0.008	0.01	—	0.04
10^{19}	2.7–3.5	2.7–3.5		2.7 3.5

layer of 1.5×10^{15} atoms/cm^3 (on a 10^{19} atom/cm^3, Au-backed substrate) yielded an etch rate of 0.89 μm per minute.

We have achieved repeatability by the careful control of various physical conditions such as total solution volume, temperature, and mix action. Muraoka et al[27] were able to improve results substantially by introducing hydrogen peroxide. We expect this preferential etch to yield suitable etch-rate ratios of at least 10:1 under the worst conditions.

8. Reduced-Height Circuits

Reduced height waveguide circuits[28-30] (Figs. 18 and 19) were used in evaluating the IMPATT diodes. The integrated heat-sink IMPATT was mounted on top of a 16-mil diameter post[31] and connected to a dc bias through a pressure-loaded pin, as shown in Fig. 18. A band-stop filter in the bias line was used to prevent rf leakage at the output frequency. At the end of the dc bias-line, an rf termination constructed of an insulating material providing high rf loss was used. Typical diode-operating conditions at above 100 GHz are V_o = 14.2 V and I_o = 111 mA. Device-circuit tuning capabilities are given in Fig. 20.

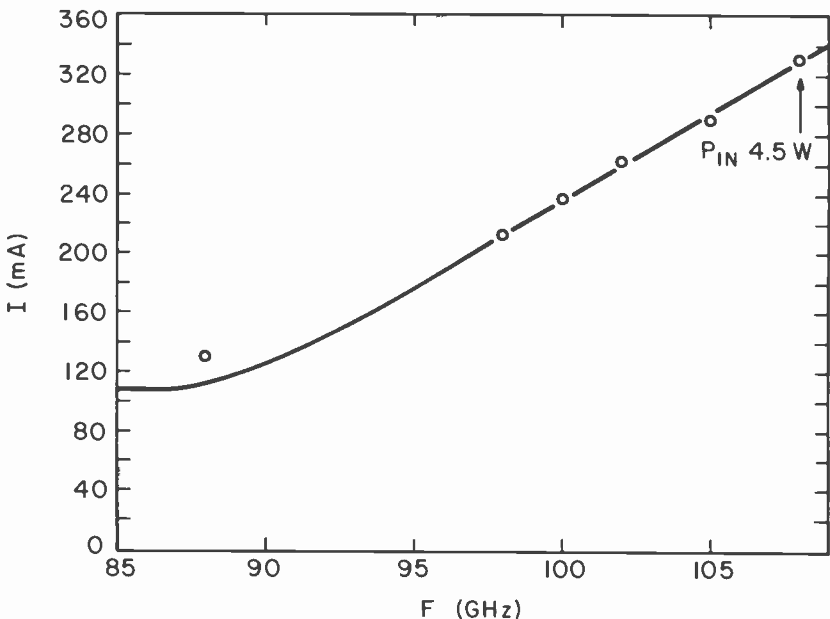

Fig. 20—DC supply current versus IMPATT frequency.

9. Hybrid-Monolithic Circuit Chip

To demonstrate the monolithic-in-silicon concept, we built a 60-GHz oscillator utilizing 5000 ohm-cm silicon wafers as our substrate. This circuit, in addition to a discrete silicon IMPATT device in chip form (Figs. 21 and 22), constitutes what we call the hybrid-monolithic source. To measure the output power of the oscillator, an E-probe microstrip-to-waveguide transition circuit was designed. Preliminary output power obtained is 6.3 mW cw at 56 GHz.

10. Conclusions

On the basis of both theoretical analyses and empirical evidence, silicon appears to be a viable material for millimeter-wave monolithic circuits when advanced device and circuit fabrication techniques are used.

The new technology which we have examined enables us to fabricate ultra thin IMPATT devices without using high-temperature epitaxy and with results that approximate those of the state-of-the-art. The basic techniques involved are (1) all ion-implantation, (2) laser annealing, (3) highly-refined SIMS profile diagnostics, and (4) novel wafer-thinning techniques. Proper application of these techniques, in addition to the propagation properties as measured on microstrip lines using high-resistivity silicon, paves the way for the development of silicon monolithic integrated mm-wave circuits.

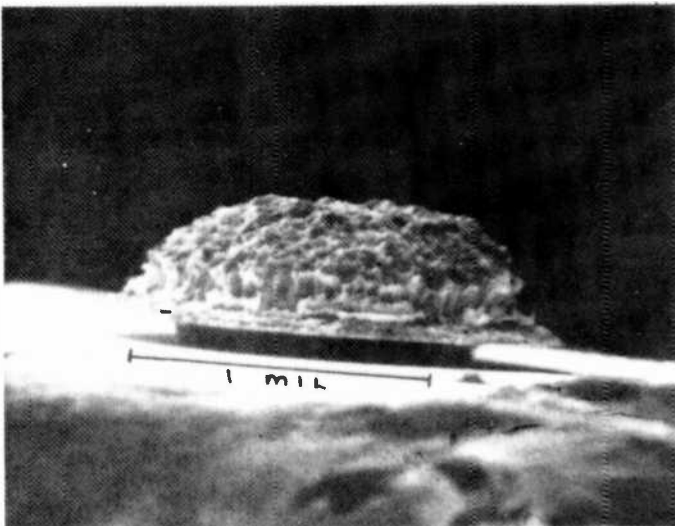

Fig. 21—IMPATT diode.

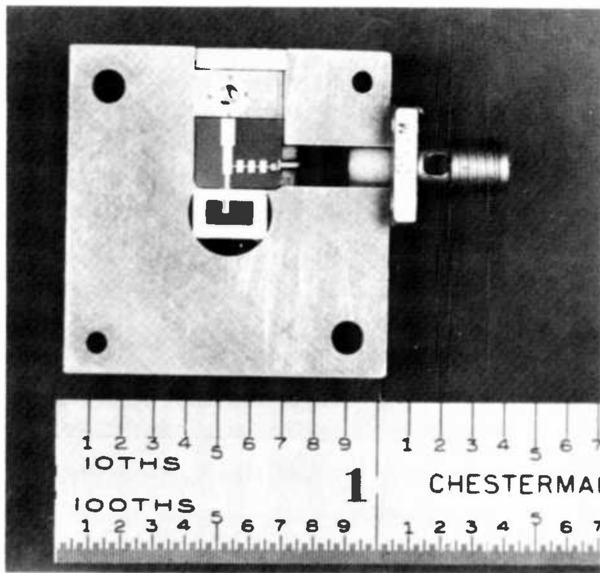

Fig. 22—Millimeter wave hybrid-monolithic circuit on silicon.

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A Low-Noise Peltier-Cooled FET Amplifier

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Abstract—Present ultralow-noise receivers in satellite-communications earth terminals use complex parametric amplifiers that are extremely sensitive to input rf drive level and pumping-frequency stability. This paper describes a development program that has demonstrated the feasibility of replacing this high-cost, complex parametric amplifier with a Peltier-cooled, GaAs FET amplifier that provides an effective noise temperature of less than 160 K (1.9 dB) over the 7.25 to 7.75 GHz band. The amplifier provides a small-signal gain of 40 dB and a gain flatness of ±0.25 dB over any 40-MHz bandwidth.

GaAs FET amplifiers are particularly suited to the use of cooling techniques to reduce noise figure, since the gain of an FET amplifier generally increases with decreasing temperature, further enhancing its performance. Moreover, commercially-available FETs and thermoelectric coolers at reasonable cost make the cooled FET amplifier approach a very attractive alternative to the parametric amplifier. The cooler control circuit described was operated from ±5-volt power supplies and provides both heating and cooling to maintain the amplifier at −20°C over an ambient temperature range of from −55 to +65°C. The container for the cooled amplifier is hermetically sealed and thermally insulated with plastic foam to maintain a frost-free environment for the amplifier circuits.

1. Introduction

Many ultralow-noise receivers for military satellite communications earth terminals for C-band operation normally use a parametric amplifier pumped by a Gunn oscillator (TEO). Such an amplifier is extremely sensitive to pump output power and frequency changes; a change in pump output power of ~0.1 dB (at the 50 mW level) causes ~0.5 dB change in rf output of the low-noise amplifier. In addition, small changes

in pump frequency compromise the noise figure and sensitivity of the receiver. Extremely tight tolerances are, therefore, required for thermal and amplitude control to meet system performance requirements. The difficulty in maintaining stable receiver operation causes many field failure problems and adds considerably to the already high costs of the parametric amplifier.

This paper describes a Peltier-cooled GaAs FET amplifier designed expressly to replace the complex and expensive parametric amplifier for satellite downlink receivers. The FET amplifier operates with an effective noise temperature (noise figure) at the terminal of less than 160 K (1.9 dB) and has an overall receiver gain of greater than 40 dB over the 7.25 to 7.75 GHz band.

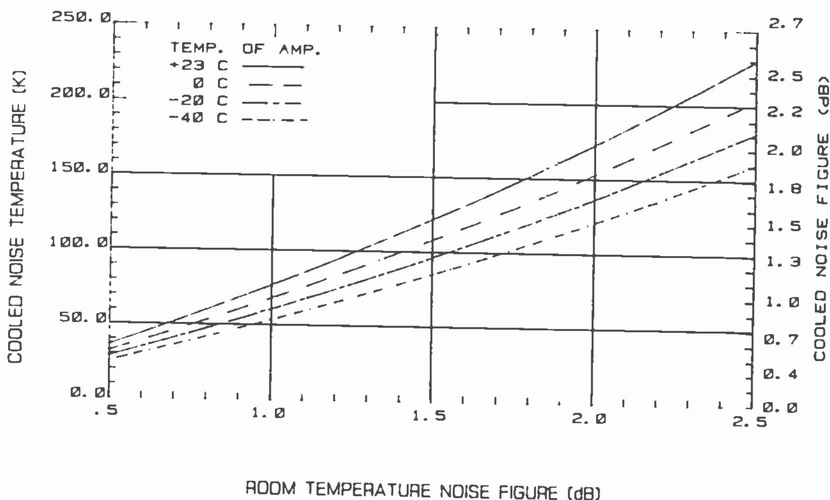

Fig. 1—Cooled noise temperature versus room temperature noise figure.

2. Developmental Approach

Recent measurements on "cooled" FET amplifiers indicate their capability to reliably replace the complex and expensive parametric amplifiers for satellite down-link receivers. GaAs FET amplifiers are particularly suited to the use of the cooling technique to reduce noise figure, since the gain of such amplifiers generally increases with decreasing temperature, further enhancing their performance. Fig. 1 shows the noise figure and noise temperature of a single-stage FET amplifier versus the room-temperature noise figure at various amplifier temperatures.[1] The

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Table 1—Specifications for Cooled Low-Noise FET Amplifier

Characteristic	Specification
Frequency	7250–7750 MHz
Bandwidth	500 MHz
Noise Temp.	160 K (max.) (1.81 dB)
Gain:	40–44 dB
Stability	±0.5 dB/8 h:ΔT = 30°C
	40–44 dB/90 days: No adjustment
Flatness	±0.25 dB/40 MHz
Intermodulation	−75 dBC with 2 carriers at −80 dBm input
Temperature	−56 to 65°C
Primary Voltage	103–132 V ac, 1 phase

availability of very low-noise FETs in the 4–8 GHz frequency range, along with the variety of thermoelectric coolers on the market, make the cooled FET amplifier approach very attractive.

The thermoelectrically-cooled FET amplifier to be described here was designed to eliminate the problems associated with the parametric amplifier, namely, extreme noise-figure sensitivity to parametric pump output power and frequency stability and associated field maintenance problems.

The development program resulted in the design of a Peltier-cooled FET amplifier that provides an effective terminal noise temperature of less than 160 K (1.9 dB) over the 7.25–7.75 GHz band with a gain of 40 to 44 dB. The initial specifications, which were essentially met by the amplifier, are shown in Table 1.

The requirements for the low-noise, ground-based amplifier necessitate operation while mounted on an antenna mast with waveguide coupling to an appropriate horn. This preserves the lowest noise figure for the receiver. The insertion loss of the interconnecting components (flange, coaxial cable, and waveguide isolator) must, therefore, be accounted for in meeting the overall terminal noise temperature of the amplifier (160 K). In addition, the amplifier must operate in an environment subject to wide temperature changes, 100% humidity, rainfall, sand storms, and other severe conditions.

3. Electrical Design

Initial effort in the amplifier design concentrated on selection of available commercial FET devices that would provide the best noise figure and gain characteristics in the 7.25 to 7.75 GHz range with suitable margin to overcome circuit losses and meet terminal noise-figure requirements.

As a result of initial measurements and characterization of available transistors, the Nippon Electric FET (type NE-13783) was selected for

Table 2—Noise-Figure and Gain Characteristics of Two NE-13783 FETs (Operating Temp. = 25°C; No Tuning)

Freq.	Low-Noise Amplifier FET Type NE-13783			
	S/N_1		S/N_2	
	Gain	NF	Gain	NF
7.1	7.9	1.64	7.9	1.35
7.5	7.9	1.52	8.0	1.08
7.9	6.4	1.28	7.1	1.00

the receiver front-end circuit. Table 2 shows the noise figure and gain characteristics of two of the amplifiers in the 7.1 to 7.9 GHz range for an operating temperature of 25°C. These measurements, taken in a 50-ohm test fixture, used biasing "tees" to simplify the circuit.

Based on these measurements, a conceptual design evolved that provided for a two-stage, ultra-low-noise amplifier to drive a post amplifier to meet the overall system gain and noise-figure requirements. The overall noise figure was required to be low enough to sustain front-end losses due to the waveguide adaptor, isolator, and a short length of coaxial cable. At room temperature, the operating noise temperature (T_{OP}) of the amplifier configuration shown in Fig. 2 can be estimated from the equation

$$T_{OP} = T_A\,(L-1) + L\left(T_{e_1} + \frac{T_{e_2}}{G_1} + \frac{T_{e_3}}{G_1 G_2}\right). \qquad [1]$$

where L is the loss of the iso-adaptor plus cable, T_{e_i} is the effective noise temperature, and G_i is the gain of the ith amplifier.

Using the measured data of Table 3, a worst case noise temperature of 177.7 K (2.06 dB) would be obtained at room temperature (T_A = 293

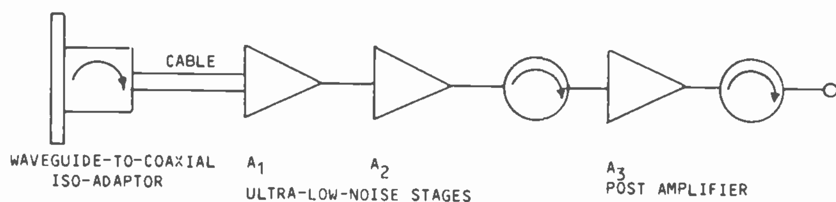

Fig. 2—Amplifier configuration.

Table 3—Measured Gain and Noise Figure Data (See Fig. 2)

Freq. GHz	Loss (L) dB	1st Stage (A_1) Gain dB	1st Stage (A_1) NF dB	2nd Stage (A_2) Gain dB	2nd Stage (A_2) NF dB	3rd Stage (A_3) Freq. GHz	3rd Stage (A_3) Gain dB	3rd Stage (A_3) NF dB
7.1	0.31	7.9	1.35	7.9	1.64	7.25	29.7	3.00
7.5	0.47	8.0	1.1	7.9	1.5	7.5	29.9	2.80
7.9	0.38	7.1	1.35	6.4	1.3	7.75	29.7	2.98

K); this is the antenna-receiver interface. In addition, the apportionment of noise figure and gain between the ultralow-noise stages and the post amplifier has enabled the consideration of tradeoffs as shown in Fig. 3. This figure indicates the minimum pre-amplifier noise figure one must obtain at room temperature to achieve an overall system noise temperature of 160 K when the pre-amplifier is cooled to −20 C and operates with a post-amplifier having the characteristics shown in Fig. 3. These data assume an overall gain (pre-amp + post-amp) of 42 dB.

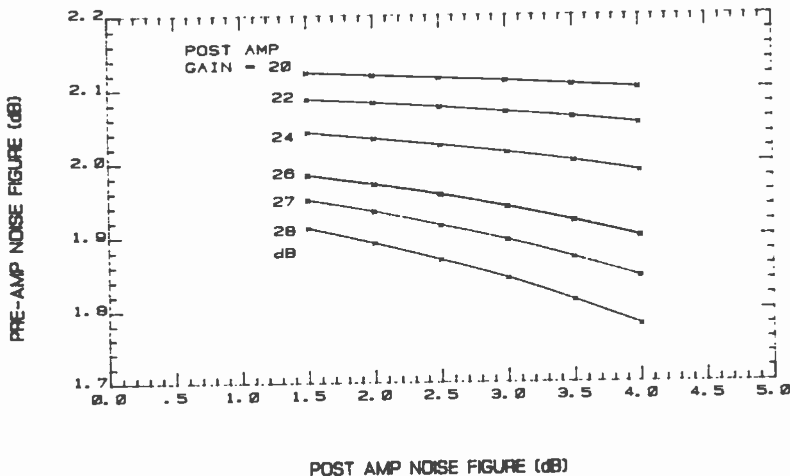

Fig. 3—Preamplifier room temperature noise figure versus post-amplifier room temperature noise figure.

To meet the designated, effective noise temperature of 160 K for the conceptual design over the operating temperature range, the first two stages comprising the pre-amplifier would have to be cooled as indicated by the relationship[1]

$$\frac{T_{n2}}{T_{n1}} = \left(\frac{T_2}{T_1}\right)^{3/2}. \qquad [2]$$

Here, T_{n2} is the effective noise temperature (160 K) at temperature T_2 and T_{n1} is the effective noise temperature at T_1 (293 K). Operation at an effective noise temperature of 160 K according to Eq. [2] requires an operating temperature (T_2) of ∼−20°C. The thermo-electric cooler for the two input stages was selected to sustain this operating temperature with an ambient temperature up to 65°C.

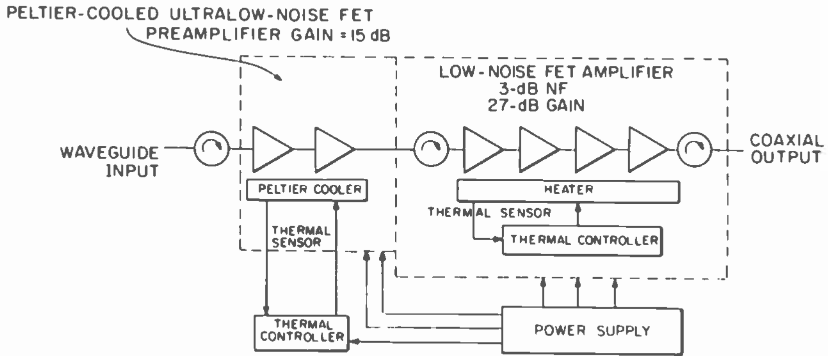

Fig. 4—Block diagram of ultra-low-noise antenna-mounted receiver.

4. Thermal Considerations

The necessity of cooling the ultra-low-noise amplifier to meet system operating specifications led to the overall amplifier design shown in Fig. 4. As indicated, the amplifier consists of a thermoelectrically-cooled, ultra-low-noise preamplifier cascaded with a more conventional FET amplifier to meet specified noise figure, gain, and gain-stabilized performance requirements. The Peltier-cooled amplifier was temperature stabilized at −20°C while the conventional post amplifier was stabilized at +70°C.

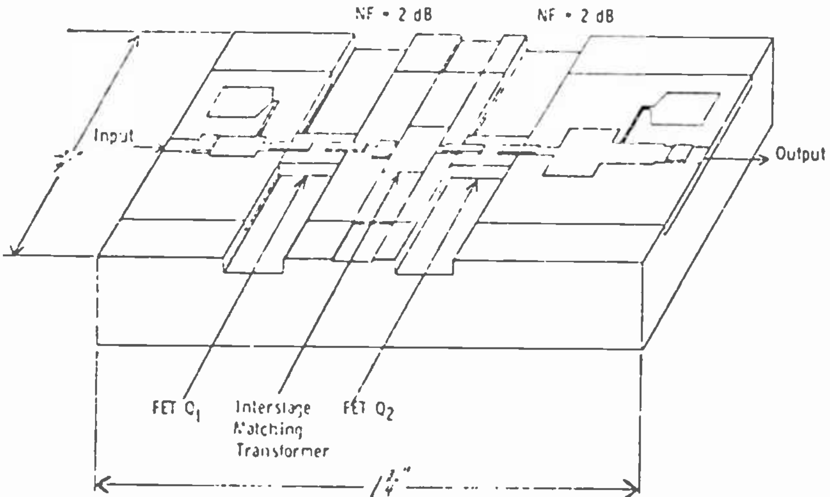

Fig. 5—Ultra-low-noise FET preamplifier.

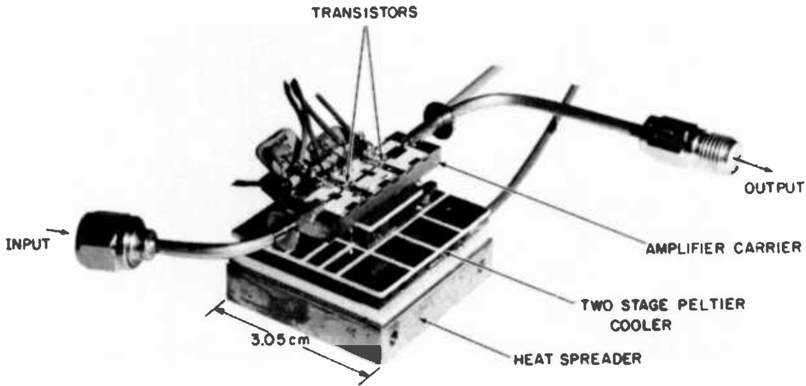

Fig. 6—Amplifier and thermoelectric cooler.

Internal sensors were used for the two thermoelectrically-cooled (or heated) stages with an appropriate feedback loop to mantain an operating temperature of −20°C over an environmental temperature of −56 to +65°C. For ambient temperatures lower than −20°C, the thermal electric "heat pump" was automatically reverse-biased to provide heating for stabilization of the system at the −20C reference temperature. For thermal efficiency, steps were taken to thermally isolate each of these amplifiers from one another as well as from the external environment.

Fig. 5 illustrates the design of the two-stage cooled amplifier. Conventional microstrip matching circuits, derived from computer-aided design techniques, were used to interface with the low-noise transistors. The alumina substrate was soldered to an appropriate metal shim designed to reduce the differential expansion over temperature extremes. Fig. 6 is a photograph of the amplifier mounted on the thermoelectric cooler.

5. Packaging

A hermetic package was required for the amplifiers to eliminate the problem of frost build-up. Although the transistors were individually hermetically-sealed, water or moisture in any form could degrade the performance of the amplifier. The final approach was to insulate the amplifier and cooler assembly and place them in a stainless-steel enclosure. The enclosure was then evacuated and back-filled with a dry inert gas and sealed. The outside of the enclosure was covered with foam insulation.

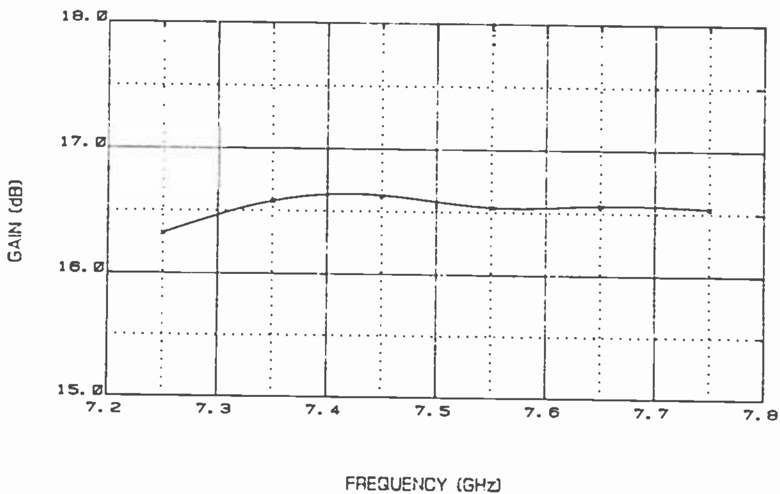

Fig. 7—Two-stage amplifier, gain versus frequency.

Thermal isolation of the amplifier was obtained by the use of low thermal-conductivity materials. For example, the input and output coaxial cable outer conductors were stainless-steel which has roughly 22 times the thermal resistance of copper. Instead of using copper wire to bring the bias voltages to the FETs, nickel wire (thermal resistance 6 times that of copper) was used between the hermetic feedthroughs and the amplifier.

6. Power Supplies

Included in the packaging were the power supplies, including control circuits, required to operate the low-noise amplifier and the cooler. This arrangement permits the system to operate directly from the single-phase, 50/60 Hz line. The supplies for the low-noise amplifiers were heavily filtered, conventional (steady-state) units, while the high-current ±5 V supplies for the cooler and control were switching power supplies chosen to keep the total power consumption low and physical size small. The switching supplies had no measurable effect on the noise figure of the system.

7. Cooler Control

The low-noise amplifier (LNA) was designed to operate at a temperature of −20°C in order to achieve the required noise figure. However, as indicated previously, the equipment will be subjected to an ambient en-

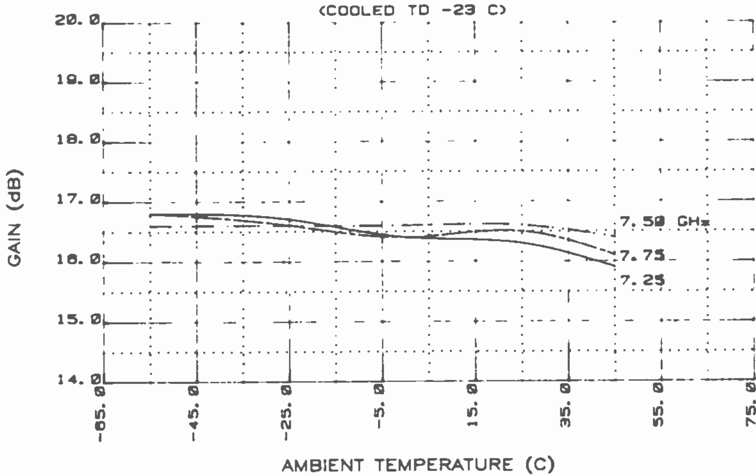

Fig. 8—Two-stage amplifier gain versus ambient temperature.

vironment in the range of −56 to +65°C. This means that heating as well as cooling is needed to maintain the amplifier at the desired temperature. Without these temperature-stabilizing processes, a constantly-changing amplifier temperature would result in constantly-changing gain and noise figure, both undesirable conditions for reliable satellite communications.

The cooler control circuit consists of a resistance bridge, with a thermistor in one arm, at the input of a differential amplifier driving a

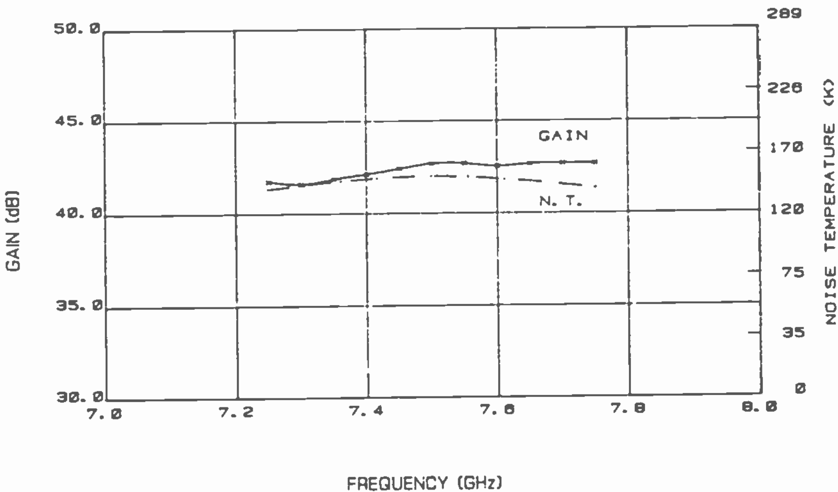

Fig. 9—Cooled low-noise amplifier. gain and noise temperature versus frequency.

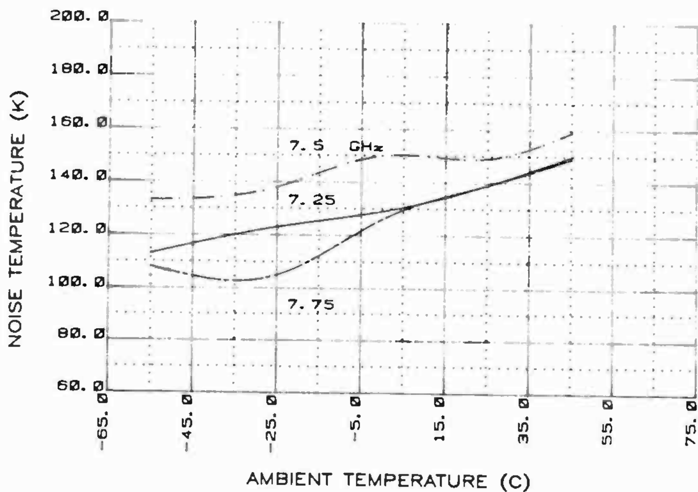

Fig. 10—Cooled low-noise amplifier, noise temperature versus ambient temperature.

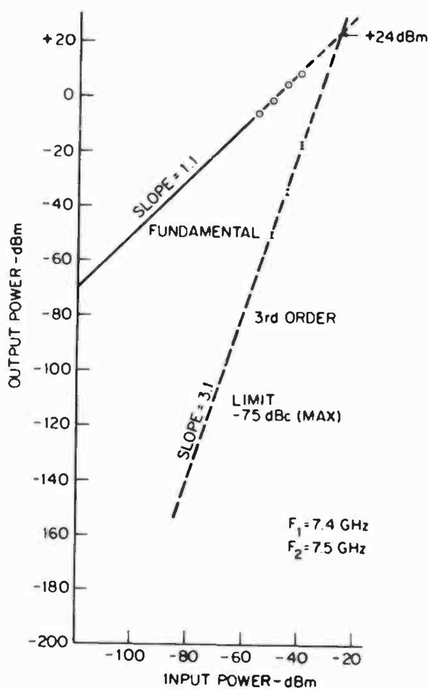

Fig. 11—Third order IMD products.

current amplifier that operates the thermoelectric cooler. When the low-noise-amplifier temperature drops below the set point, the direction of the current flow to the cooler is reversed, providing heat to the LNA to maintain stable performance.

8. Results

The gain of the two-stage, preamplifier over the 7.25 to 7.75 GHz band is shown in Fig. 7. The room-temperature noise figure is less than 2.1 dB (180 K) over the band. Cooling the preamplifier to −23°C resulted in a 1.8 dB (149 K) noise figure. Fig. 8 shows the gain versus ambient temperature of the cooled preamplifier at three frequencies in the band.

Fig. 9 shows the system gain and noise temperature versus frequency in a room-temperature ambient. The system noise temperature versus ambient temperature at three frequencies in the band is shown in Fig. 10.

The third-order, intermodulation products are shown in Fig. 11. These data were taken at a drive level of −50 to −40 dBm with two equal-level carriers 100 MHz apart. The curves were extrapolated from the measured points to the −80 dBm input power level. The third-order IMD products were well below the −75 dBC maximum level of the specification.

This program demonstrated the feasibility of replacing a parametric amplifier with a Peltier-cooled, low-noise FET amplifier for mast head operation in the 7.25–7.75 GHz band.

Acknowledgments

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Solid-State Ku-Band Radar*

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Abstract—The development of rf and i-f components for a Ku-band pulsed radar, as well as the construction and tests of this radar, are described. The developed components include an FET oscillator, FET power amplifiers, a biphase modulator, a low-noise amplifier, and charge-coupled (CCD) signal correlators. The radar transmits a 32-bit biphase coded pulse at a power of 350 mW. The receiver uses a 3-stage, 27-dB-gain amplifier chain with a 6.9-dB overall noise figure. The compact binary-analog signal correlators use 64-stage charge-coupled devices to process receiver I and Q channels. The radar gave excellent performance during ranging tests using a Doppler simulator and digital FFT processor.

Introduction

There is an ever-increasing need for highly mobile air- and ground-based tactical radars. These systems must be lightweight, compact, rugged, and efficient. To be effective they must operate with a low probability of being intercepted. This leads to the use of low-peak-power, long rf pulses.

This paper describes the component development for a small, lightweight Ku-band radar. These components include a mechanically tuned

* The work reported here was sponsored by the U.S. Army Electronics Research and Development Command, Fort Monmouth, NJ, under contract number ERADCOM DAAB07-78-C-2435.

oscillator, a biphase modulator, FET power amplifiers, a low-noise FET amplifier, and charge-coupled signal correlators. In addition, pulsers and code and sync generators were developed to permit operational tests of the radar system. Despite the long rf pulses, the spatial resolution was kept high by a digital pulse-compression technique. The subsequent experimental evaluation of this system confirmed the basic feasibility of a solid-state Ku-band radar employing state-of-the-art GaAs FETs for rf amplification and CCD correlators for digital pulse compression.

To orient the reader, a short description of the radar layout is given. The components are then discussed, and the assembled radar's performance is described. Ranging tests using Doppler simulators and external FFT (Fast Fourier Transform) processors were developed to provide quantitative radar sensitivity data. These signal processors and resulting data are also discussed.

2. Radar System Configuration

The main objective of the radar assembly was to provide a means for the testing and demonstration of the developed components. The specific configuration shown in Figs. 1 and 2 was designed to be flexible, constrained only by a few performance objectives such as a 12-km maximum range capabilty, a range resolution of 50 m, and the use of a pulse compression scheme. The choice of pulsed over cw operation was based on a desire to use a design approach leading to a future compact radar including a single antenna for both transmitting and receiving. In cw op-

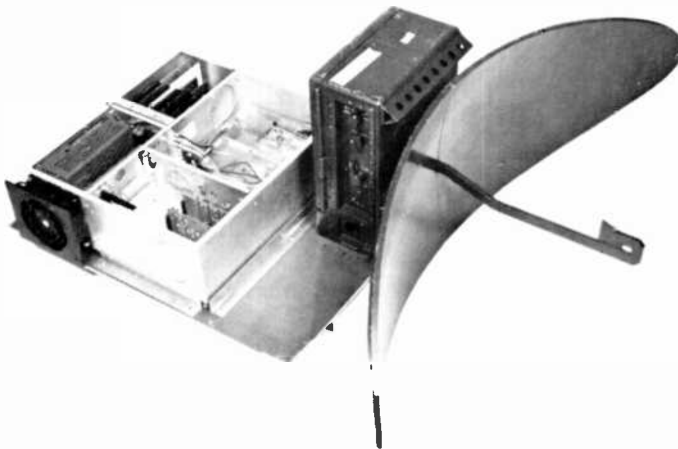


Fig. 1—Photograph of Ku-band radar.

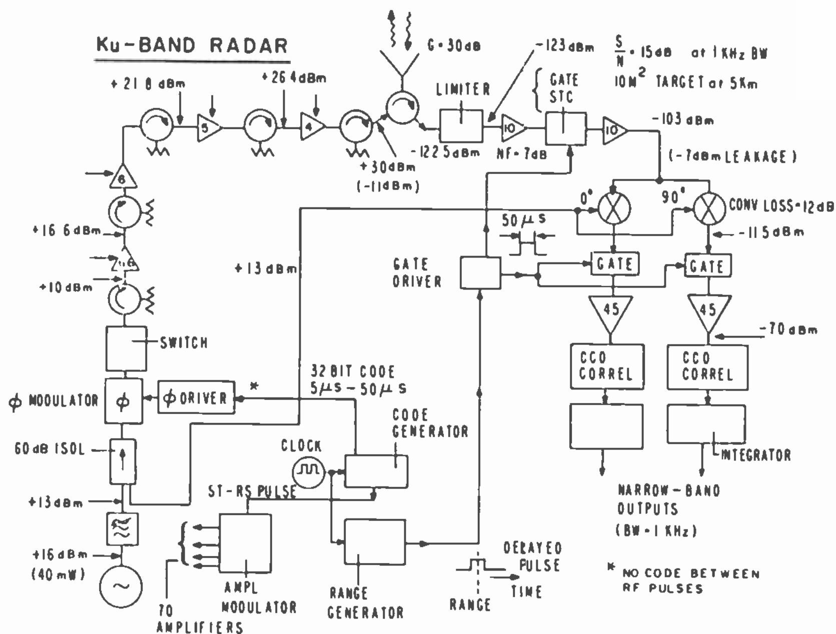


Fig. 2—Block diagram of Ku-band radar.

eration, the low isolation of a monostatic antenna would most certainly produce saturation of the low-noise receiver.

It was also desirable to provide coherent transmit and local oscillator sources so that the I (in phase) and Q (quadrature) outputs from the system would be suitable for Doppler processing. The most straightforward form of coherent detection is to use a homodyne configuration where a sample of the unmodulated transmit power serves as the local oscillator source. The degradation caused by the close-to-carrier $1/f$ noise is kept negligible by amplifying the received signal through a high-gain (27 dB) low-noise amplifier (LNA). This approach, not convenient when implemented for instance with low-noise TWTs or parametric amplifiers, is quite practical now because of the availability of low-noise GaAs FETs.

The transmitter consists of a mechanically tuned oscillator followed by a phase shifter (modulator) and three FET amplifiers. The received signal is amplified by a 3-stage low-noise FET amplifier and mixed with the local oscillator (LO) in a quadrature i-f mixer. The I and Q video signals are amplified and correlated with the transmitted pulse. The correlator outputs are evaluated directly or digitized and Doppler processed.

3. RF Components

3.1 Power Amplifier

The transmitter power amplifier chain consists of three cascaded amplifiers with intermediate isolators. The first two amplifiers are similar, and are designed for the FET type MSC 88101 (Microwave Semiconductor Corp.). The third amplifier features higher power and is designed for the FET type MSC88102.

The design of these power amplifiers started by characterizing the FETs under both large- and small-signal conditions at frequencies between 16.0 and 16.5 GHz. The large-signal measurements were carried out with the aid of a computer-controlled tuner (load-pull) connected at the output of the device to be tested. These measurements determine the optimum load impedance which allows the device to deliver the maximum output power. The results for the higher power device, type MSC88102, are shown in Fig. 3. The gate voltage, adjusted for maximum output power, corresponds to a drain current that is approximately one-half of the saturated current at zero gate bias I_{DSS}.

The data of Fig. 3 were used to design an output circuit that closely

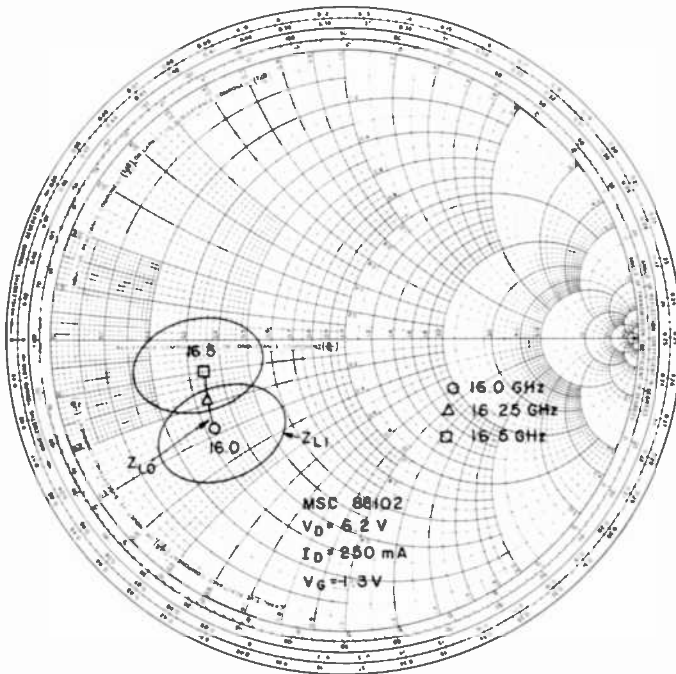


Fig. 3—MSC 88102 optimum load impedance.

approximates the optimum load impedance Z_L. The small-signal S parameters of the device were then used, in conjunction with the optimum load impedance, to determine the input matching circuit that provides the highest uniform gain over the operating bandwidth. This procedure takes advantage of the fact that the input impedance of the device is rather insensitive to the level of the rf power. The result is a design optimized for output power as well as for gain.

The input matching circuit is designed as a two-section impedance transformer, where the first section is printed on a 10-mil-thick Cuflon* substrate having a dielectric constant of 2.1, and the second section is printed on a 10-mil-thick alumina substrate. The use of the two different substrates reduces the discontinuity between the two microstrip lines. The tuning circuit at the output of the FET is a single-step transformer printed on a 10-mil-thick Cuflon substrate.

The power performance was measured for 3 stages cascaded with intermediate isolators. The maximum output power at 16.25 GHz is 350 mW, with a gain of 15.8 dB, and an efficiency of 10%. The small-signal gain is 17.5 dB. The 350-mW output power is obtained at 1.7 dB of gain compression.

3.2 Phase Shifter

Two types of reflection-mode phase shifters were considered, one using a varactor and the other a PIN diode, as the phase-controlling element. The advantage of a PIN diode phase shifter is that it can be designed to operate over a broad bandwidth. This is generally desirable, although not of paramount importance in our case, since the required bandwidth is only 3%. A problem of the PIN diode phase shifter, however, is that during the transition from a low- to a high-resistance state, the diode impedance goes through a value that substantially matches the source. At this point, little power is reflected by the PIN diode and therefore little power is transmitted through the phase modulator. Since the receiver phase detector is also sensitive to the amplitude of the received signal, this large increase of insertion loss during the phase transition time can decrease the system sensitivity.

Alternatively, a varactor phase shifter uses a mainly reactive controlling element whose insertion loss does not change greatly during the phase transition. In addition, a varactor phase shifter has the significant advantage of requiring low drive power. However, it has typically a narrower band, although some tradeoff can be made between insertion loss and bandwidth.

* Polyflon Corp., New Rochelle, NY.

For the above reasons, a varactor phase shifter was chosen for this radar. The basic components are shown in the schematic of Fig. 4. The varactor capacitance C_v varies between 0.2 and 0.9 pF as the bias is varied between 0 and −30 V. The inductor, L, tunes the minimum value of C at approximately the center of the operating bandwidth, while the matching circuit provides the impedance transformation required to produce the 180° phase shift over the operating bandwidth. The elements C_b are 30-pF MOM (metal-oxide-metal) capacitors and are used as dc blocks. The varactor bias V_v is applied through the inductance, L, without the need of rf chokes. The absence of rf chokes leads to a very high speed modulation capability.

The matching network was built using microstrip lines printed on a 10-mil-thick Duroid* substrate having a dielectric constant of 2.3. The low dielectric constant makes this material well suited for high-frequency operation. The varactor, in chip form, was mounted directly on the metal base and was connected to the circuit by means of two bond wires. The tuning inductance, L, was printed on the Duroid substrate and was connected to the MOM capacitors by bond wires.

The measured phase shift as a function of varactor voltage showed a quite uniform phase-shift step (180° ± 6) over the frequency range from 16.0 to 16.5 GHz. The insertion loss as a function of the phase shift, including the circulator loss of approximately 0.5 dB, is shown in Fig. 5. The optimum range, for which the insertion loss at the two extremes of the 180° phase-shift step is equal, starts at 11° and ends at 191°. The corresponding insertion loss at the two extremes is 2.6 dB and reaches a value of 4 dB during the transition.

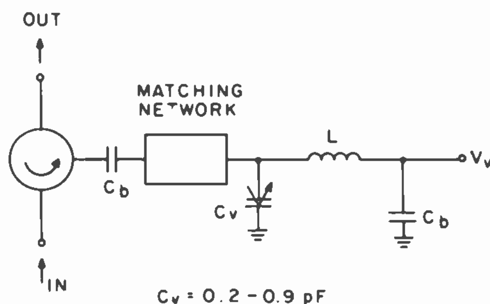


Fig. 4—Schematic of phase shifter circuit.

* Rogers Corp., Chandler, AZ.

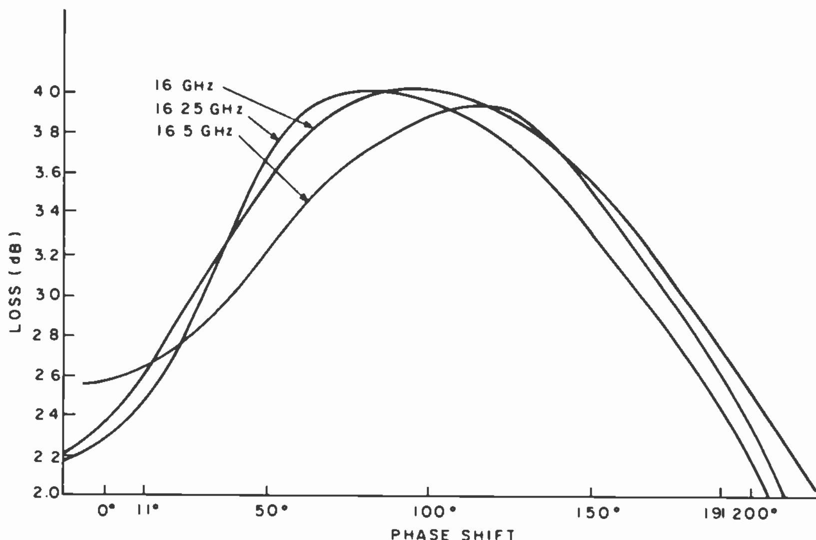


Fig. 5—Insertion loss versus phase shift.

3.3 Oscillator

Two types of solid state sources—Gunn and FET oscillators—were considered suited for this radar system. The Gunn oscillator is a well established source of microwave power. Typically it features low noise, good tunability and simple mechanical construction due to the use of a two-terminal active device. It is inefficient, however, which could be a drawback in systems having a limited source of dc power, such as battery operated radars. The FET oscillator is much more efficient—often by a factor greater than 10. However, its noise performance was not well documented in the literature, specifically in comparison with the Gunn oscillator. The only available informal reports that were available from other researchers indicated a surprisingly high noise in FET oscilators. In view of these factors, both Gunn and FET oscillators were designed and tested, with the intention of using an FET oscillator only if its noise could be reduced to be similar to that of a Gunn.

The circuit we selected for the FET oscillator is shown schematically in Fig. 6. The FET is an MSC 88101 that is operated in a grounded-drain configuration by reversing the bias of this regular grounded-source device. This configuration, made possible by the inherent symmetry of a GaAs FET, maintains the desirable internal feedback characteristics of a common gate device, without the disadvantage of requiring a special device.[1,2]

The frequency controlling element in this circuit is a coaxial resonator

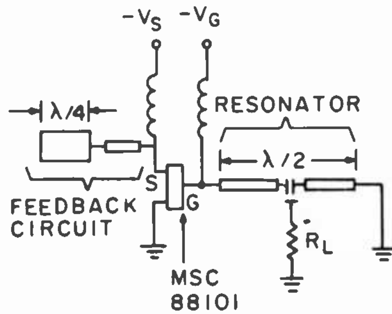


Fig. 6—Schematic of FET oscillator.

approximately λ/2 long with a 20-pF dc blocking capacitor located at the center. The output load R_L is coupled by means of a small capacitive probe protruding into the cavity. The feedback circuit is realized by a small section of transmission line printed on Duroid substrate that provides reactive loading of $+j45$ to $+j50$ ohms over the frequency range from 16.0 to 16.5 GHz.

The circuit selected for the Gunn oscillator is shown schematically in Fig. 7. The Gunn diode (MA 49126-118) is mounted in a cavity built using a WR 42 copper waveguide. The cavity, approximately λ/2 long, is bounded on one end by a waveguide short and on the other end by an iris. The waveguide short is placed at a λ/4 distance from the diode post. The cavity is tuned by a sapphire rod protruding into the cavity at the point of highest electric field. The output power from the oscillator is coupled through the iris into a waveguide to coaxial transition, which is built as an integral part of the oscillator.

A summary of the performance of the FET and Gunn oscillators is shown in Table 1. For similar levels of output power, the FET is more efficient than the Gunn oscillator by a factor of 10.7. In certain cases, this large difference in efficiency can be important, specifically when the overall system performance has to be weighed against the overall dc power consumption.

The external Q of the circuits (Q_{ex}) was measured by injection locking

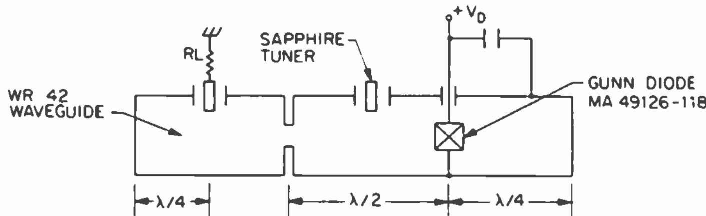


Fig. 7—Schematic of Gunn oscillator.

Table 1—Summary of Performance of FET and Gunn Oscillators

	Power (mW)	Efficiency (%)	Q_{ex}	FM Noise (Hz)	AM Noise (dB_c)
FET	69	14	21	100	−124
Gunn	55	1.3	1300	<30	−114

the oscillator by an external source. As shown in Table 1, the Q_{ex} of the FET oscillator is far lower than that of the Gunn. However, when the output load and the FET were decoupled from the resonator in an attempt to increase Q_{ex} (and therefore improve the oscillator frequency stability) the operation became unstable for Q_{ex} approximately greater than 100. This was traced to spurious resonances being activated in the coupling circuit between the FET and the resonator. We found that it was difficult to avoid spurious resonances and, at the same time, to achieve at these high frequencies the loose coupling between the FET and the resonator that is required for high Q operation. Many of the reports of excessive noise in FET oscillators may derive from the difficulty of achieving high-Q coupling between the FET and the resonant cavity.

The FM and the AM noise of the oscillators were also measured. Table 1 lists the data measured in a 100-Hz bandwidth set 10 KHz away from the carrier. The FM noise, expressed here in rms frequency deviation, is much higher in the FET oscillator than in the Gunn oscillator. The noise differs by more than 10 dB, although an exact comparison could not be determined because equipment limitations prevented an accurate measurement of the very low noise level of the Gunn oscillator. This difference, however, is not unexpected considering the large difference in Q_{ex}.

The AM noise, also shown in Table 1, is expressed as the noise to carrier ratio in dB. This noise is 10 dB lower for the FET oscillator, which is a most interesting result since the AM noise is essentially independent of the Q of the circuit. This result indicates that the FET is a low-noise device and that the high FM noise of the FET oscillator is probably caused only by the low Q of the circuit. The low AM noise of the FET oscillator indicates also that for similar circuit Q values, the FET oscillator might provide an even lower FM noise than the Gunn oscillator.

Full optimization of the FET oscillator for low FM noise could not be completed within the scope of this program. Therefore, the Gunn oscillator, which gave better FM-noise performance, was chosen as the primary source for the experimental radar implementation.

3.4 Low-Noise Amplifier

The low-noise amplifier is part of the receiver and precedes the quadrature mixer. It consists of a chain of three separate stages directly cascaded to form a high-gain, low-noise unit. The first two stages use single-gate FETs because they provide the best noise figure available at Ku-band (short of using complicated and expensive parametric amplifiers). However, the gain of each stage is not very high, typically only 6 dB, and therefore the second-stage contribution to the overall noise figure is significant. This is why the first low-noise stage was followed by a second low-noise stage using the same type of device.

These two stages are then followed by a third stage, featuring a dual-gate FET. While this stage has a higher noise figure, it also has much higher gain. Some of this high gain is regenerative which requires special precautions, such as close connection to the proceding stage and an output isolator. An important feature of the dual-gate FET stage is the availability of gain control, obtained by changing the bias voltage on the second gate. RF power leakage into the receiver during the transmit cycle can saturate the receiver or, for very large leakage, even damage the front end. Both problems are circumvented here by pulsing the drain voltages of the FETs, which turns the receiver off during the transmit time. This prevents the receiver (particularly the video amplifiers) from saturating and, at the same time, protects the front FET from possible burnout due to excessive leakage. This arrangement simplifies the system and eliminates the need for a limiter whose loss would increase the noise figure by approximately 0.5 dB.

Overall, this amplifier is an interesting unit, useful in many systems. It features high gain, low noise, a sufficiently large bandwidth, a gain control useful for sensitivity time control or for automatic gain control, and very rapid drain-bias pulsing.

The first two stages are essentially identical amplifiers built with Plessey GAT5 FETs. These devices, featuring a 2-mm diameter ceramic package, were characterized at Ku-band by *S*-parameter measurements. The circuit was initially chosen to match the input and output impedance of the device and was then optimized for minimum noise figure. The circuit was fabricated using mirostrip lines printed on a 10-mil-thick Cuflon substrate.

The last stage of the low-noise amplifier uses a dual-gate FET of type NE46300 (Nippon Electric Co.). This device was purchased in pellet form and was mounted on a special carrier. A low-inductance rf ground is provided for the second gate by a 30 pF MOM capacitor of small physical size (0.76 × 1.5 mm) mounted adjacent to the pellet.

The circuit design is oriented toward high and uniform gain over the

500 MHz bandwidth. Minimization of the noise figure was not considered important here because this stage was preceded by the two low-noise stages. The circuit was printed on a 10-mil-thick Cuflon substrate.

The three stages were directly integrated in a small metal housing (5.0 × 2.8 × 2.5 cm) together with a resistive voltage dividing network that feeds the appropriate bias voltages to the gates of the three FETs.

The measured frequency response is shown in Fig. 8. The gain is 27 to 28 dB from 16.0 to 16.5 GHz. This gain is unusually high for an amplifier featuring only three stages. The gain is also controllable over 25 dB by biasing the second gate of the third stage from 0 to −2 V. The noise figure is 6.9 dB and is practically constant over the operating bandwidth.

4. Low-Frequency Components

4.1 Code and Sync Generator

The biphase modulated pulse is used with a receiver correlator to provide pulse compression ratios that are proportional to the number of code bits used. The "0" and "1" bits correspond to the 0 and 180° phases of the transmitted signals. (The binary/analog correlator is discussed later.) A binary rather than higher order phase code is used, since higher order codes greatly increase the amount of hardware without significantly reducing the correlation side lobes. A digital generator producing a serial binary sequence provides the necessary code. The radar uses a 32-bit code length, which is compatible with the commercially available signal correlator included in this system. Each bit is 200 ns long. Since there is no singularly optimum 32-bit code, such as the 7- or 13-bit Barker codes,[3] it was considered useful to include a provision for varying the code so that side-lobe levels can be evaluated for various codes.

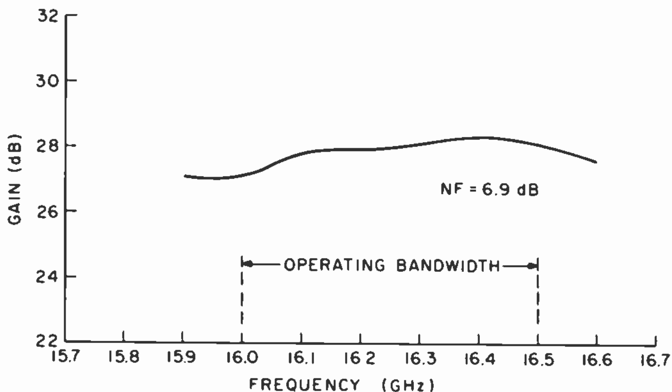


Fig. 8—Low-noise amplifier gain versus frequency.

A single clock frequency is used for the time-keeping function in both the long coded and short uncoded pulse modes. A 10-MHz clock is used because the correlator circuitry requires an input frequency that is twice the bit rate. It is also a convenient choice since the short uncoded pulse length (200 ns) is the same as a single bit length. The resulting 32-bit pulse therefore becomes 6.4 μs long. The typical maximum operating range for tactical radars is between 10 and 50 km. For convenience, the pulse repetition period (51.2 μs) was chosen to be a binary multiple (×8) of the coded pulse length corresponding to an unambiguous range of approximately 12 km.

A functional block diagram of the sync and code generator circuits is shown in Fig. 9. These circuits generate the appropriate logic levels to drive the pulsers for the receiver and power amplifiers. The power amplifier chain is activated during the transmit period and the low noise amplifiers are activated during the receive period. When operating in the coded pulse mode, the 32-bit code is programmed by DIP type SPST switches, each providing a "Hi" or "Lo" state that is sequentially tapped by a multiplexer. In the long pulse mode, the phase of the rf reflects the multiplexed DIP switch settings during the transmit time. The phase shifter then remains at 0° during the receive period. The phase shifter also remains unmodulated throughout the entire short-pulse operating mode while the power amplifiers are activated for a period approximating one bit length.

The static shift registers (SSR) of the CCD correlator must be programmed with the transmit code before the received signal can be correlated. The maximum shift-rate capability of 1 MHz is significantly

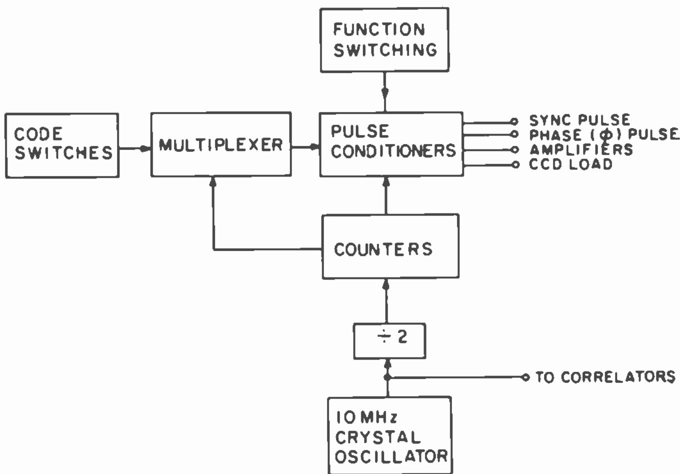


Fig. 9—Sync and code generator.

slower than the clock frequency. The clock frequency is therefore divided down to 50 kHz and supplied to SSR clock inputs on both of the *I* and *Q* CCDs. When a "Load" button is pushed, a single in-sequence 32-bit code, which is timed with the SSR clock output, is loaded into the CCD static shift registers. The process ceases after the last bit is scanned and normal operation again resumes when the button is released.

4.2 Video Amplifiers

The *I* and *Q* outputs from the quadrature mixer must be amplified to levels sufficiently high for use in the CCD correlators. The system design requires nominal video gain of 50 dB and a bandwidth that is wide enough to cover the majority of frequency components present in the typical 32 bit, 200 ns per bit code. Two amplifier stages are used: a first stage having an equivalent input noise to 5 μV at 16 MHz followed by a second stage featuring a two-pole amplifier-filter. The combined bandwidth of 4 MHz, which is conservatively wide for this application, is determined by the second stage-feedback elements.

4.3 Signal Correlator

The original radar system design included a pulse compression scheme using a section of an RCA binary/analog charge-coupled device (CCD) for signal correlation. The available devices had code-length capabilities of 128, 256, and 512 bits, which would provide more pulse compression than planned (originally 25 bits) and, combined with the 10 MHz maximum bit rate, would result in a prohibitively long minimum range. Also it was not possible to foreshorten the code lengths since there were no available intermediate tap points. Since the system coding was to be biphase-binary, the Reticon R-5401 32-bit binary/analog bucket-brigade device was chosen. This device includes a 64-stage tapped analog delay line. The sampled analog signal is point-by-point shifted and multiplied with the binary code that is stored in the static shift register (SSR). The device output is the sum of the products of the discrete analog samples and corresponding binary weights. The analog output of a single correlator resulting from the binary code being fed directly into the correlator analog input terminal is shown in Fig. 10. The binary code (top trace) and the correlated output (lower trace) is shown for this ideal test. The particular code chosen for this test provides side-lobe levels of approximately −11 dBc. There are numerous code combinations that will provide similar side-lobe performance since there is no singularly optimum 32-bit code.

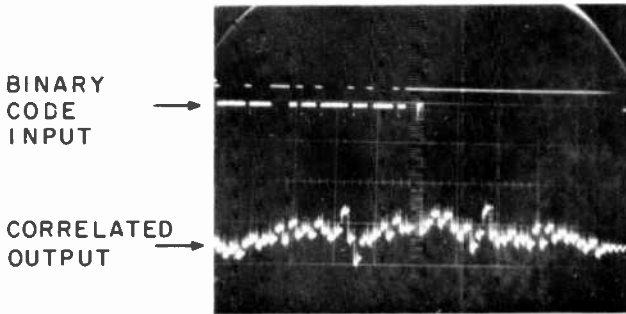
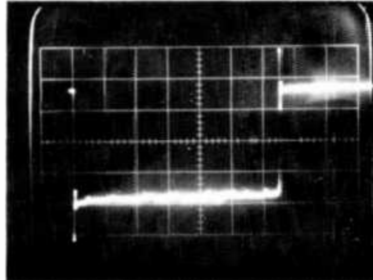


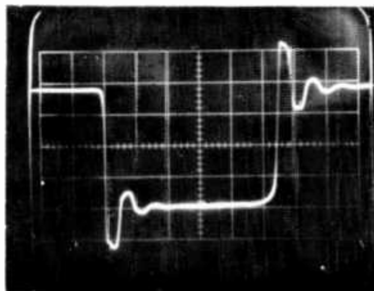
Fig. 10—Correlator output using binary code input.

5. Radar Evaluation

The completed radar was bench tested and checked initially with an uncalibrated target. The bench tests included rf output measurements in both the long and short-pulse modes. Fig. 11 shows the systems' rf output monitored by a crystal detector. The irregularities in the amplitude of the long pulse output are caused by phase modulator losses that occur during the transitions between the 0 and 180° states. The



LONG RF PULSE (1μs/div)



SHORT RF PULSE (50 ns/div)

Fig. 11—RF output of radar.

crystal detector output exhibits an overshoot, as can be noticed in both operating modes. The pulse rise and fall times are typically 5 and 7 ns. The short pulse is stretched from 200 to 270 ns by a flip-flop in the code generator circuit that extracts a single pulse.

Initial radar ranging tests were conducted using an elevated water tank for the target. The tank is located at a known range of 1.9 km but is of unknown cross section. An oscilloscope display of a single correlated output channel is shown in Fig. 12. The photograph shows side lobes associated with the target as well as other targets at closer range. Fig. 13 shows the video amplifier output for this same target using the short-pulse noncorrelating operating mode. The correlation gain cannot be accurately determined from these tests.

A digital Doppler signal processing test bed (Fig. 14) was assembled by RCA Missile and Surface Radar and used to evaluate the radar's performances. The test bed performs a Fast Fourier Transform (FFT) using the radar's video or correlator targets mounted on a 60-meter tower at a range of 1.6 kilometers. The analog I and Q outputs are converted to a digital format consisting of 8-bit words which are stored in a 4K, 16 bit memory. It was necessary to limit the range window so that the data

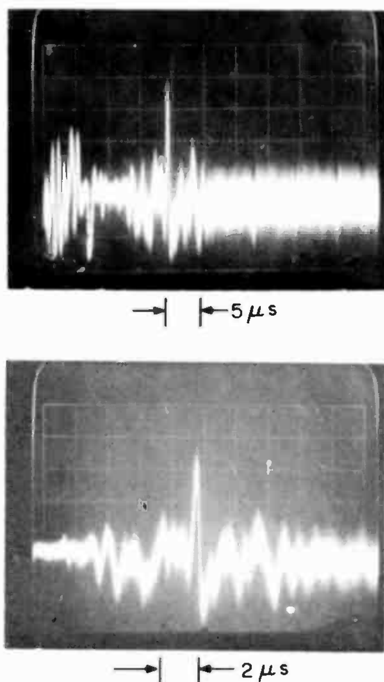


Fig. 12—Correlator output (water tank target).

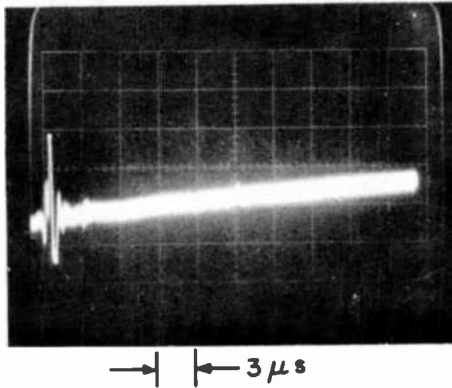


Fig. 13—Video amplifier output with target.

from 1024 dwells necessary for a 1024-point FFT would fit into the 4K of memory. The range gate width is therefore limited to one sample.

Eight separate groups of 1024 samples are recorded at random times to increase the chances of "catching" a maximum signal return from the spinning doppler simulators. Processing of target data was performed on a PDP-1103 interfaced to a JP-1350A graphics display. The 1024 point FFT. The magnitude of each FFT output point was taken and the results converted to dB with the maximum set at 0 dB. The points were then stored on disk and tape files. A reformatting program was run to convert the plot points to Calcomp format on disk. The resulting file could be displayed on the graphics display through a program which

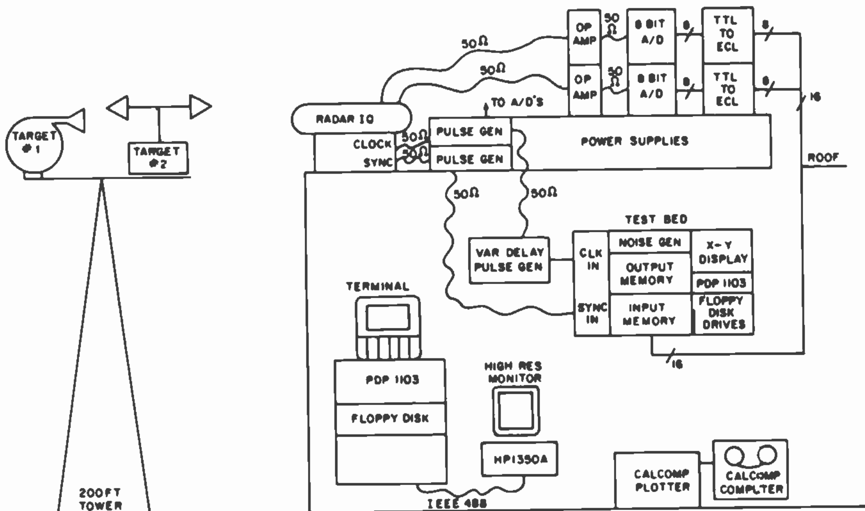


Fig. 14—Radar test bed.

converts Calcomp format to HP-1350A format. The Calcomp file could also be transferred to tape and plotted on the Calcomp plotter.

Fig. 15 shows a plot of a typical Doppler spectrum for the two targets using the CCD correlators within the radar. The two targets have different cross-sections and opposing velocities. The target-to-tower signal ratios were artificially increased in these figures to minimize non-linear saturation effects in the CCDs and video amplifiers due to the strong tower signal. This was accomplished by directing the center of the antenna's main lobe above the tower's top. The S/N of the target signals is therefore degraded by approximately 6 dB. A calculation of the expected S/N for target 2 while on antenna bore sight is 49 dB, which compares fairly well with the off-bore-sight measurement of 38 dB.

A second set of tests was performed to evaluate the radar's performance using computer correlations. For these tests, the radar's video outputs were digitized and fed directly to the computer. It was necessary for the computer correlation run to take 32 samples for each dwell resulting in a full 4K memory after 128 dwells. A 128 point FFT was then calculated. For comparison, a 128 point FFT was also run using the Radar's CCD correlator outputs. The results showed equivalent Doppler S/N for both cases. This demonstrated very satisfactory performance of the CCD correlators.

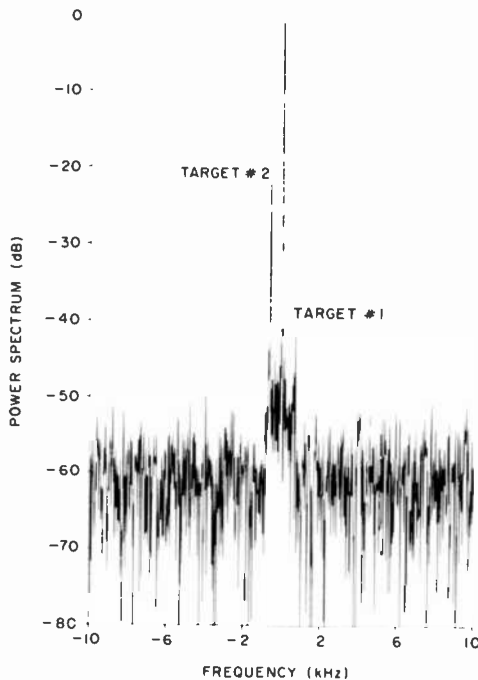


Fig. 15—Doppler spectrum using CCD correlated output (128 point FFT).

6. Conclusions

The application of new techniques to the development of a Ku-band phase-coded pulsed radar has been successful. State-of-the-art GaAs FETs were used for rf amplification throughout the radar, for both power amplification in the transmitter chain and for low-noise amplification in the receiver chain. Direct amplification of Ku-band frequencies by these high-frequency devices has definite advantages over the low-frequency amplification and varactor multiplier approach. The system is simpler to construct, as well as to align, and can be built in a smaller size. In addition, a new technology, being developed in our laboratory based on lumped–element microwave circuits batch-fabricated on BeO substrates, will eventually allow us to build the entire rf section in a very small size and at low cost.

The radar was designed for high spatial resolution by means of digital pulse compression using a 32-bit binary-phase modulation scheme. Charge-coupled devices were used in the receiver for signal correlation. These binary/analog devices are ideal for this application since they are small, light, and have low power consumption compared with the usual correlator circuitry. The maximum data-shift rates of 5 MHz provide a range resolution of approximately 50 m. The speed of future devices is anticipated to increase and at present already exceeds 10 MHz.

The homodyne configuration chosen for the radar resulted in a simple system that, because of the single rf source, does not require complex shielding and rf filtering. The radar features a peak output power of 350 mW over a 6.4 μs pulse and is equiped with a 30-dB antenna. It was evaluated on a test range using a 0.4 m^2 Doppler target situated 1.6 km away. The Doppler frequency was clearly identified and the nominal signal-to-noise ratio was 38 dB.

Because of the recent advances in GaAs FET technology, output powers of several watts will become feasible. In addition, improvements in low-noise GaAs FETs will lower the noise figure to approximately 4 dB. These results have already been obtained in the laboratory. Thus, in the near future, a similar system could have a figure of merit approximately 14 dB higher than that of the present system, thereby greatly increasing its versatility.

Acknowledgments:

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Varactor-Tunable, High-Q Microwave Filter*

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Abstract—The selectivity of tunable microwave filters that employ varactors as the tunable element is limited by circuit and varactor losses. A tunable resonant element is described in which these losses are compensated by the negative resistance of an FET circuit. Experimental performance results are shown for single and two-section bandpass filters using these elements.

Introduction

In commercial and military microwave systems there has been an increased demand for the inclusion of electronic controls in components, and in many of these systems the speed of control is an important consideration. In a tunable high-Q filter, the function to be controlled is the resonant frequency of one or more elements within the filter. Presently, the magnetically tuned YIG element is most commonly used in microwave applications. The high-Q of YIG resonantors assures high selectivity, but tuning speed is limited to the millisecond range by the magnetic tuning circuit. Varactors, which are frequently used in resonators at UHF frequencies, can be tuned at rates that are about three orders of magnitude higher than those of the YIG, but their relatively high losses severely limit selectivity in passive circuits at microwave frequencies.

It has been shown[1,2] that the inherent varactor losses can be compensated by the negative resistance of an active element. We choose a

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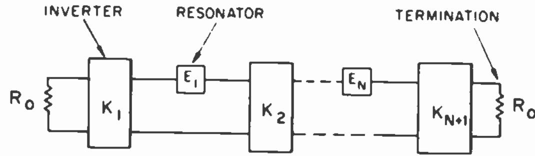


Fig. 1—Block diagram of multi-section bandpass filter using impedance inverters.

GaAs FET to provide this negative resistance because of its known broadband capabilities. This paper describes how the negative resistance of the FET, the varactor, the necessary tuning inductance, and dc connections are combined on a suitable carrier into a resonant element, and how these elements are then employed in single- or multi-section bandpass filters using standard passive coupled-resonator filter design considerations.[3-5]

Resonant Element Design

Fig. 1 shows a multi-section bandpass filter in its basic form. The N resonant elements E are connected as shown via $N+1$ coupling networks K to the terminating impedances R_o. The coupling networks are designed to have impedance transforming properties to give required N-section filter response. The resonant element E in its ideal form can be represented by the equivalent circuit diagram shown in Fig. 2. The varactor and its losses are represented by the capacitor C_v and the resistor R_v, respectively. The FET with its feedback configuration is represented by the impedance Z which has a negative real part. The inductor L_T finally brings the combination of all parameters into resonance.

The major components of the resonant element are the varactor and the negative resistance circuit. The most important varactor parameters are junction capacitance (C_j) variation with bias voltage, breakdown voltage, and series resistance. These parameters are rather predictable and depend upon varactor construction.[6] The particular varactor chosen

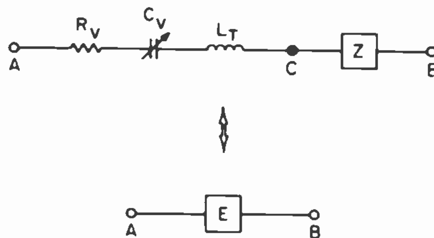


Fig. 2—Idealized equivalent circuit of active resonant element.

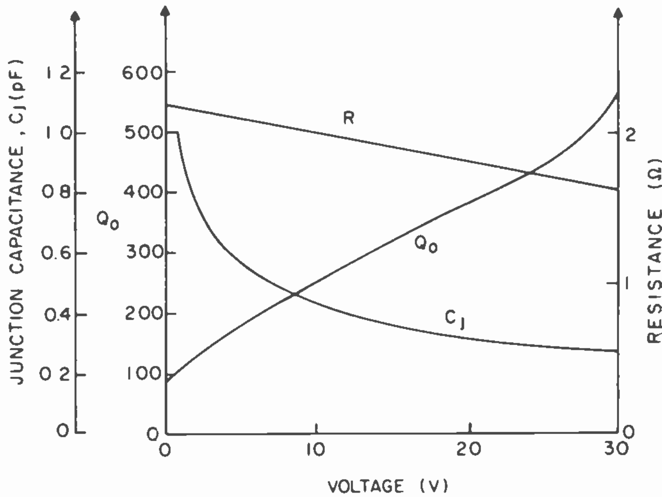


Fig. 3—Varactor characteristics.

for this program was an inexpensive abrupt-junction Si-varactor in chip form with a capacitance ratio that is larger than 6:1 between 0 and 30 V ($C_{j(0)}$ = 1.42 pF, $C_{j(30)}$ = 0.22 pF). Fig. 3 shows the measured junction capacitance and series resistance of this varactor. The series resistance was derived from Q measurements at 1 GHz. Since diode Q varies inversely with frequency, the need to overcome all or most of the varactor losses (1.5 to 2.5 Ω) at frequencies near 10 GHz for high-selectivity applications is evident.

The objective of the negative resistance FET circuit is to attain an impedance element with a negative real part of 1.5 to 2.5 ohm. This objective was met with an FET in the arrangement shown in Fig. 4. The circuit element values were chosen to operate the FET in a common drain configuration, which provides negative resistance over a larger range of frequencies than other configurations.

Calculations for the impedance between terminals C and B of Fig. 4 without the capacitor C_F show that this FET circuit can be represented

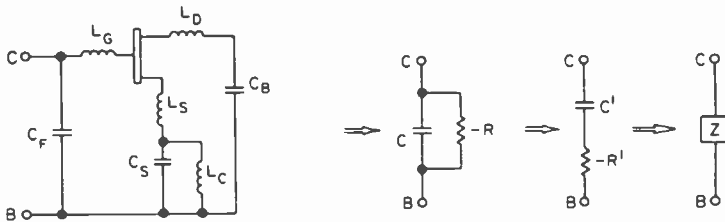


Fig. 4—Equivalent of negative-resistance-producing FET circuit.

by a parallel circuit of a relatively large negative resistance (50–200 ohm) and a small capacitance (~.07 pF).

The capacitor C_F, therefore, serves two purposes. It Q-transforms the negative resistance to a series value in the desired range and it also prevents effective capacitance ratio reduction of the varactor, which eventually has to be placed in series with the FET circuitry, as shown in the element diagram of Fig. 2. The results of a sample calculation for the complete circuit of Fig. 4 in the 7 to 12 GHz frequency range is shown in Fig. 5 for two values of C_F (0.4 and 0.6 pF).

The varactor and the negative resistance circuitry are combined on a common carrier to obtain a series-resonant high-Q element that serves as a building block for multi-section bandpass filter designs. The carrier must have small parasitic effects upon resonance and permit easy access to the required external bias and tuning voltages. Fig. 6 shows a realizable assembly of the resonant element that fulfills the essential carrier requirements. The varactor, the negative resistance circuit, and the tuning inductance are fabricated on an alumina wafer. Metallic thin-film circuits support the varactor, the FET, and all associated circuit components. Wire bonds representing lumped-element inductors are used to interconnect the individual components. Also shown in Fig. 6 is an electrical equivalent circuit of this element.

This realization differs electrically from the ideal element representation in Fig. 2 by the carrier-pad capacitances C_2 to ground of the metallized alumina wafer, which make it a four terminal structure. The capacitances C_2 are absorbed into the coupling networks of the filter. This realization provides good electrical symmetry and requires only one FET and one varactor per element. A true series resonance is es-

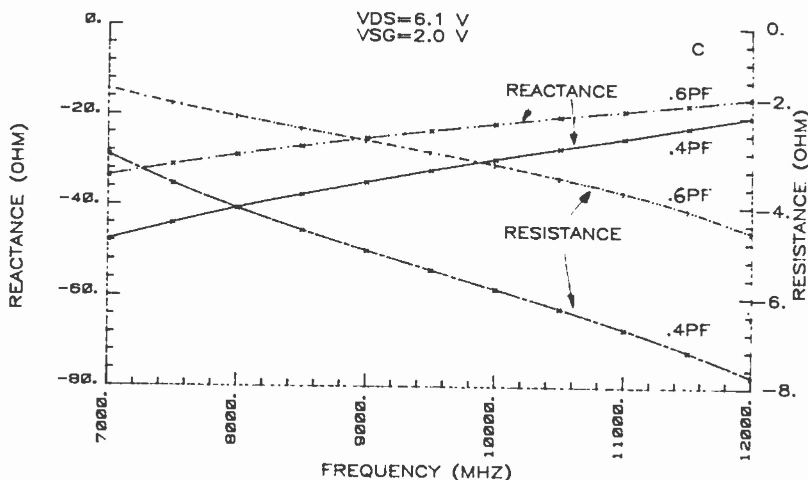


Fig. 5—Calculated FET impedances.

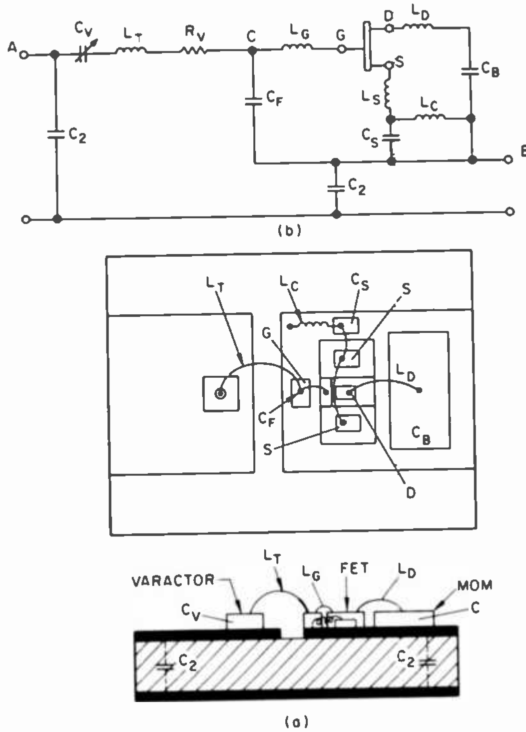


Fig. 6—Resonant element construction: (a) realizable configuration and (b) equivalent circuit.

tablished when one considers that the parasitic pad capacitances C_2 of the carrier can be absorbed by necessary inverters. The negative resistance element between the terminals B and C in the diagram was realized electrically as shown in Fig. 4 and described above. A 0.38 mm thick 5 × 5 mm alumina substrate was chosen as the carrier material. Metallic thin-film technology was used to print onto the carrier the supporting pads for the varactor, the FET circuit, and high-impedance choke lines. The FET and varactor circuits mounted atop the pads are essentially isolated from carrier ground. The carrier and rf by-pass capacitors are attached to a 10 × 5 × 1.5 mm flange and in this form represent the basic filter building block in modular form.

Experimental Element Evaluation

The performance of various individual elements was evaluated in a single-section-filter test fixture (shown in Fig. 7). This fixture contains two 50-ohm line sections terminated by Type-SMA connectors. The

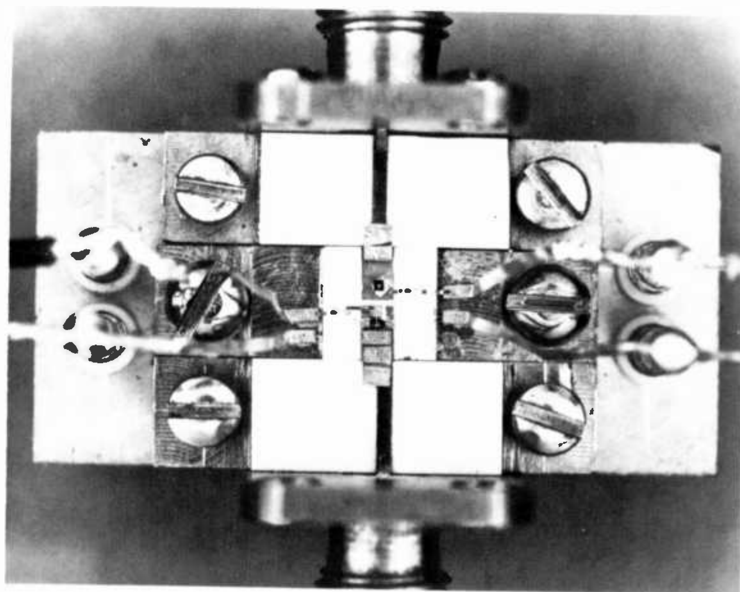


Fig. 7—Element test fixture.

element is capacitively coupled to these lines via adjustable tabs. The capacitance of the tabs to the line together with the pad capacitance C_2 of the carrier represents the inverter sections necessary for bandpass filter operation. Flying leads connect to stand-offs, over which the required dc voltages for varactor and FET are applied. In the following paragraphs, various performance aspects of a single-element filter section are highlighted.

Selectivity

The selectivity of a bandpass filter is definable by the 3-dB bandwidth and the transmission rejection as a function of frequency. The rejection is mainly determined by the basic filter design (number of elements, response shaping, etc.). The 3-dB bandwidth, on the other hand, is a function of the resonator parameters (slope parameter and Q) and the external loading (determined by the coupling). The unloaded Q of the resonator can be adjusted over a wide range with the gate voltage of the FET. The range of adjustments is limited by the occurrence of instabilities. The coupling at input and output is adjustable via the proximity capacitance between the gap of a tab, which extends from each end of the resonator, and the printed conductor of the 50-Ω line sections. This range of adjustments is also limited by stability considerations.

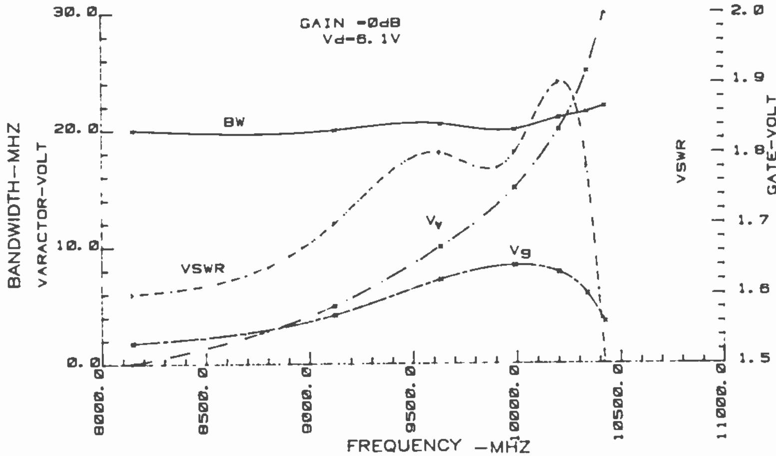


Fig. 8—Measured 3-dB bandwith, VSWR, gate and varactor voltage of high selectivity single-section filter.

Fig. 8 shows the measured results of an element with fixed coupling to assure stability while maintaining a 0-dB transmission loss over the tuning range. The 3-dB bandwidth, VSWR, gate and varactor voltage are shown as a function of midband frequency. The frequency is adjusted by varying the varactor voltage and adjusting the gate voltage at each setting to result in a 0-dB transmission loss. The feasibility of uniform 3-dB bandwidth (20 ± 1 MHz) with fixed coupling is demonstrated over a 2300-MHz tuning range.

Tuning Range

The tuning range is a function of the capacitance ratio of the varactor between useful minimum and maximum varactor voltage limits and of other capacitive reactances in the resonator proper that affect this ratio. These unwanted but unavoidable reactances are introduced by the carrier, the interconnections between components, and the FET circuit; they effectively reduce the capacitance ratio and, with it, the tuning range. A varactor with high cutoff frequency (high-Q) and large capacitance ratio is best suited for broadband tuning. The reactance of such varactors is high, and the series resistance is low. Although the varactor and the FET chosen in the experiments were not fully optimized, the frequency deviation over which the elements were tunable while assuring stability and adequate selectivity was typically 2.5 GHz in the 7 to 11 GHz frequency range. The 3-dB bandwidth varied between 20 to 40 MHz over the tuning range.

Signal Input Effects

It was observed that power input affects the filter response. Generally the transmitted power is reduced and midband frequency shifts as input power is increased. Gain reductions for a fraction of a decibel can be observed with power inputs as low as −15 dBm, noticeable frequency shifts of a few megahertz occur at −10 dBm. It was also observed that the effect is a function of element loading; we suspect that the rectified rf voltage at the gate junction of the FET is producing power-dependent variations of negative resistance and reactance sufficient to cause the changes observed in selectivity and transmission. The response of a tightly coupled element with a 3-dB bandwidth of 95 MHz was evaluated at three different input power levels. As shown in Fig. 9, for a 20-dB input level change from −30 dBm to −10 dBm, the center frequency shifts by less than 10 MHz, the midband loss increases by 1.2 dB, and the 3-dB bandwidth increases by 5 MHz, from 95 to 100 MHz.

The effects of power input from two signals upon filter performance were briefly observed. With the filter adjusted as shown in Fig. 9, the observed amplitude and frequency shifts were about the same for a combined power input as for a single signal. The third order intermodulation for two equal-amplitude signals in the passband ($\Delta f = 15$ MHz) as a function of the power input of each signal is shown in Fig. 10. The IMD product decreased while one signal remained in the passband and the difference frequency was increased. The power input of the second

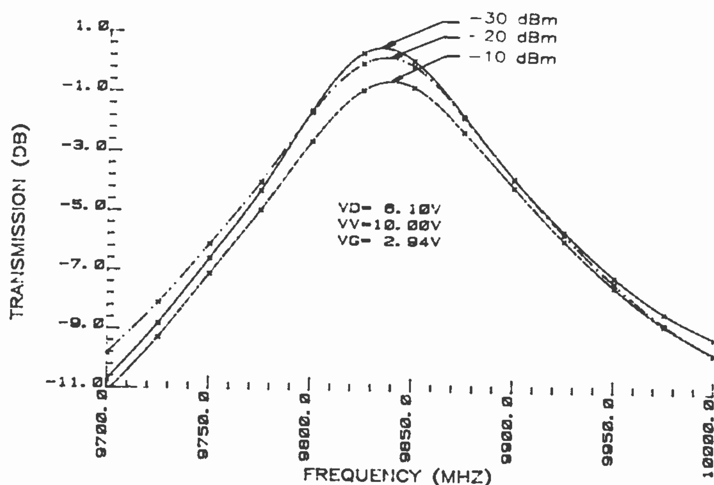


Fig. 9—Measured transmission response of single section filter for three input power levels.

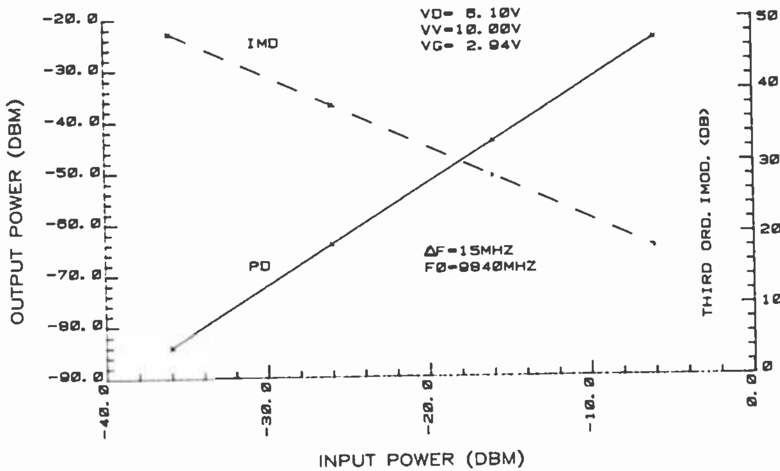


Fig. 10—Measured two signal intermodulation distortion as a function of input power level.

signal at the response skirts was also increased to give identical power outputs of the two signals; no third order distortions above −80 dBm were observed when the inband signal was −27 dBm and the out-of-band signal +6 dBm with a signal separation of 200 MHz. However, as total power output of the two signals was increased, response shifts were about the same as for a single signal at a comparable power output.

Noise Figure

Transmission loss in the active filter can be kept small and with some operating voltage adjustments can even turn into gain. As with other active components, however, output noise is a limiting factor and noise figure is an appropriate measure of performance. The noise figure is increasingly important in high sensitivity applications and those requiring large dynamic ranges. The plot in Fig. 11 shows measured noise figures for a single-section filter over the 8.9 to 10.4 GHz frequency range. At each measurement the filter was adjusted for 0-dB transmission loss. The relatively large values of noise figure, ranging from 16 to 20-dB, were neither expected nor is their reason presently fully understood. We expected the noise figure to be somewhat larger than that for an amplifier with the same FET, which is rated 4-dB at 10 GHz, since the FET loading is far from the optimum noise impedance values. Apparently the feedback configuration is responsible for an additional increase in the noise figure. Additional efforts on noise limitations and noise figure reductions are required.

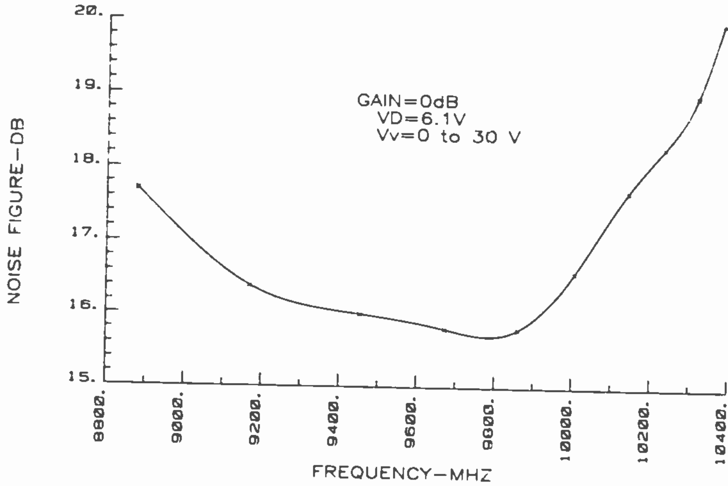
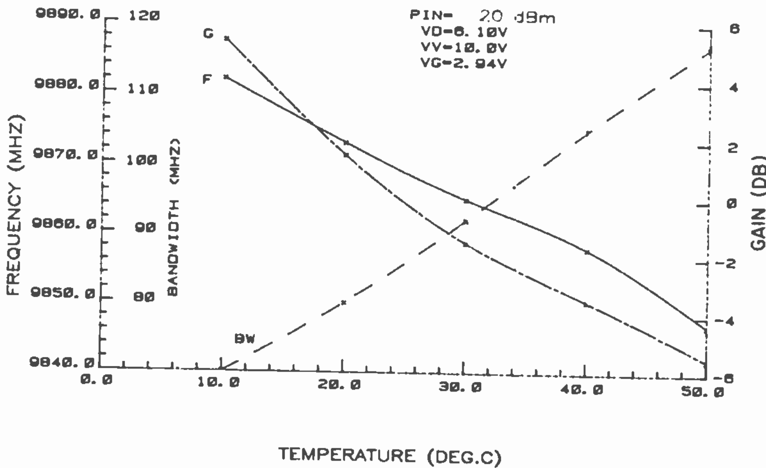


Fig. 11—Measured noise figure at different frequency settings.

Temperature Effects

The major effects of temperature upon filter performance are caused by the temperature sensitivity of the varactor and the FET. This sensitivity changes the reactance and the negative resistance within the resonator. The temperature sensitivity of a single resonant element is shown in Fig. 12. With the operating voltages and the rf-drive level kept constant and the temperature varied between 10° and 50°C, the center frequency decreased by about 930 kHz/°C and the 3-dB bandwidth in-



TEMPERATURE (DEG.C)

Fig. 12—Measured effects of temperature on 3-dB bandwidth, midband frequency, and transmission.

creased by 1.1 MHz/°C. The midband transmission decreased by nearly 0.2 dB/°C at the higher test temperatures and about 0.75 dB/°C at the lower temperatures. These relatively large changes suggest the use of temperature controlled operation or the use of voltage control that compensates partially for temperature changes.

Tuning Speed

The frequency tuning of the filter depends upon accurate tuning voltage settings to attain a predetermined response at a predetermined frequency. The number of variable voltages in the worst case are $2N$, where N is the number of elements in the filter. The number of variable voltages is reduced in cases where the voltages of individual elements track. The necessary voltages are attainable using microprocessor control and preprogrammed voltage look-up tables. The microprocessor addressing system activates the appropriate driving circuitry for the filter. The tuning speed of the filter is determined by a combination of addressing system access time, slewing and settling times of the driving system, and the time constants of the varactor and gate circuits. The ultimate speed of the operational filter will depend mainly on the addressing and driving circuits since the time constants in the experimental element are only about 100 ns. These time constants, if need be, could be further reduced by altering the decoupling resistors in the dc lines and by reducing the values of the feedthrough capacitors.

Two-Section Filter

The development of the filter element described above led to an element design that promises a high degree of success for constructing filters with extended tuning bandwidth. Two elements to be used in the construction of a two-section filter were fabricated in modular form as outlined in the previous sections. Each element was tested and adjusted individually in a test fixture shown in Fig. 7. The aim of the adjustments was to bring frequency, selectivity, and tuning voltages into a common range so that the maximum frequency range would be attained when combining two elements into a two-section-filter arrangement.

The two-section filter consists of two modular elements that are capacitively coupled at input and output to short 50-Ω microstrip transmission lines that terminate in SMA connectors. Coupling between elements is also via capacitive proximity. Capacitive feedthroughs provide access to the dc connections necessary for filter operation. A metallic partition between elements with an iris around the coupling tabs prevents both uncontrolled coupling between elements and waveguide

resonances of the 38 × 35 × 20 mm brass enclosure that would cause spurious rf feedthrough. Fig. 13 shows an overall view of a completely assembled filter with partitions in place but with cover removed.

Adjustments of the filter are first made with the cover and the partition removed. These adjustments entail capacitance changes obtainable from the coupling tabs that extend from each end of each resonant element and appropriate voltage changes. The operating voltages of the two elements are adjusted to correspond approximately to those observed previously for each element at the same frequency within the tuning band. Keeping the two voltages of one element fixed, slight adjustments of the other voltage pair are made while observing the swept response of the filter on a network analyzer. Voltages are adjusted for best transmission response. The coupling to the transmission lines and the tabs between elements are adjusted next, until a true, well matched, maximally flat response with desired 3-dB selectivity is obtained. Coupling adjustments are limited by stability considerations and also have to be touched up subsequently to correct for effects caused by the partitions and the cover. It was found that coupling adjustments first made at the upper-frequency end of the filter tuning band resulted in better filter operation over the entire band. This also avoids instabilities that tend to occur at the high-frequency end.

The filter was evaluated while maintaining the case temperature at 23°C ± 0.5°C by means of a circulating bath controlled heatsink. Fig.

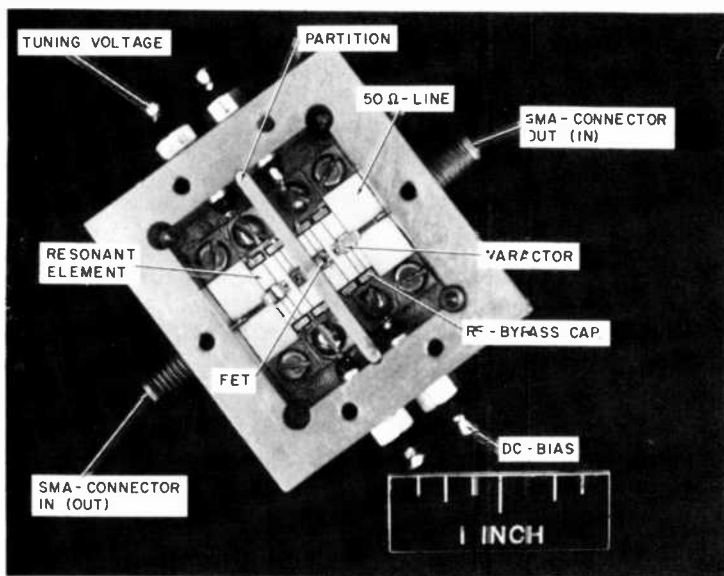


Fig. 13—Final two-section filter.

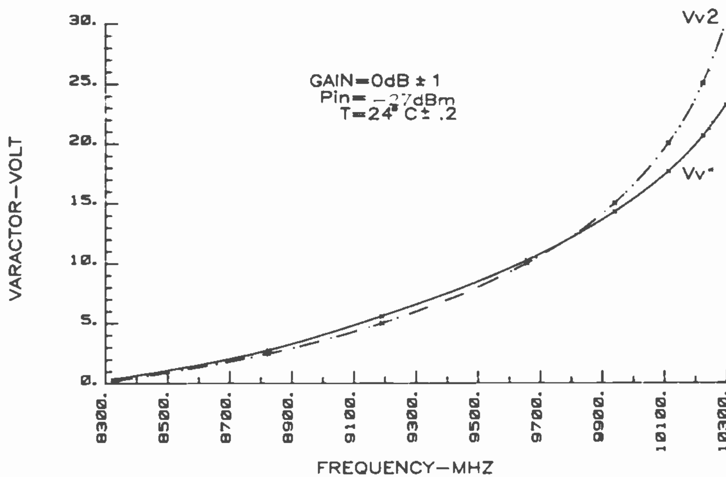


Fig. 14—Measured varactor voltage versus midband frequency of two-section filter.

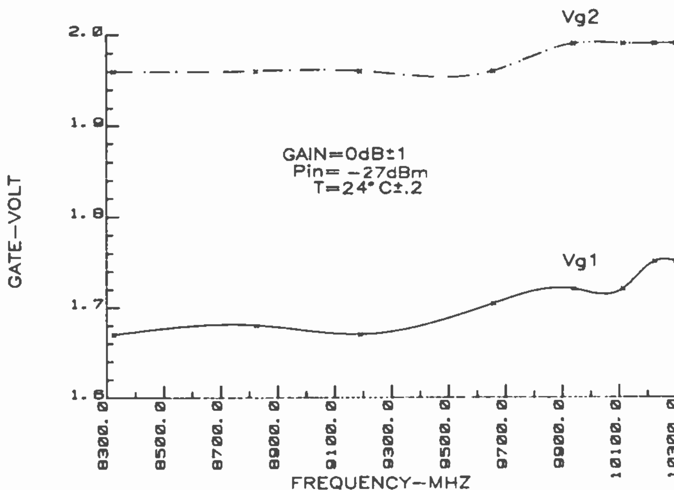


Fig. 15—Measured gate voltages versus midband frequency of two-section filter.

14 shows the varactor voltages and Fig. 15 the gate voltages, both versus frequency for a 0-dB transmission adjustment. The maximum tuning range of 2.0 GHz is determined by the mutually inclusive frequency range of the two elements in the 0- to 30-V tuning range of the varactors. As shown in Fig. 16, the corresponding 3-dB bandwidth over the tuning band varied between a low value of 34 MHz at the frequency of 9.66 GHz, and 39 MHz at the frequency of 10.3 GHz. The bandwidth variations are mainly a function of varactor Q, a value that is about four times larger at the high frequency than at the low frequency. The coupling also varies

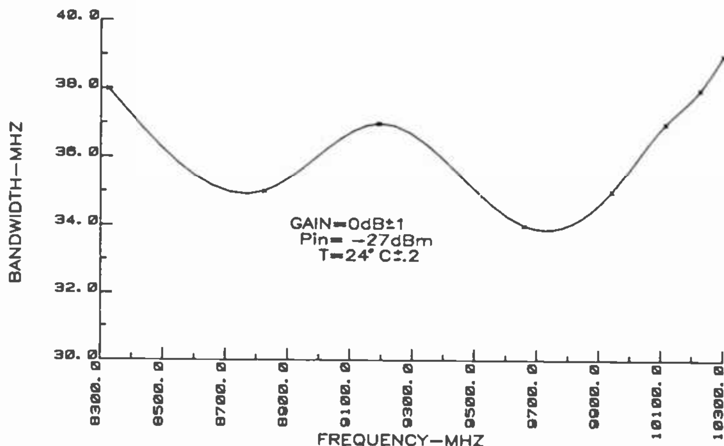


Fig. 16—Measured 3-dB bandwidth versus midband frequency of two-section filter.

as a function of frequency, but its effect upon bandwidth in this case is a compensating one.

More detailed response results were obtained on the automatic network analyzer. Fig. 17 shows the transmission response at a particular set of voltages for both the forward and reverse directions of power flow. The corresponding phase responses and group delays in the passband are in good agreement with expected values for a two-section filter. The response symmetry with respect to power flow is good. The effects of power input variations were also observed and are similar to those shown in Fig. 9 for a single section filter. A slight shift in midband frequency, a widening of the response, and a fall-off in relative transmitted power were noticeable.

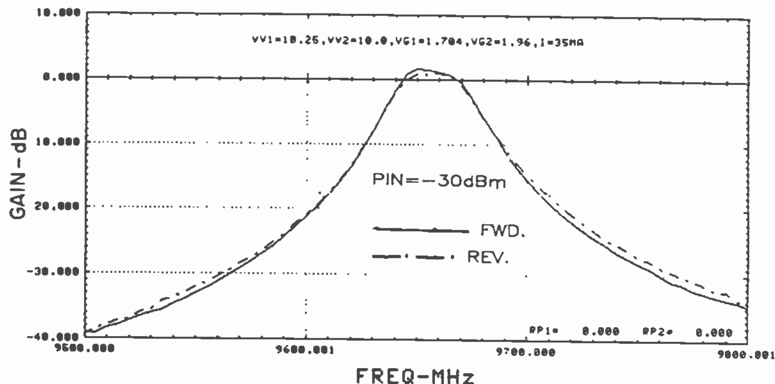


Fig. 17—Measured transmission passband response for forward and reverse power flow of two-section filter.

Noise figure evaluations over the entire tuning band resulted in values of 24 ± 1 dB. These values of noise figure, even though high, are close to what can be expected in view of the values for the individual elements.

The performance of the two-section filter can be summarized as follows:

Midband Frequency, F_o	8.3 to 10.3 GHz
3-dB Bandwidth, BW	36 ± 4 MHz
Midband Insertion Loss, L	0 dB ± 1 dB
Rejection, F_o ± 2BW	24 dB
Noise Figure, NF	24 ± 1 dB
Power Input	<−10 dBm
Tuning Voltage	0–30 Volt
Size	38 × 35 × 20 mm

Conclusion

A method to overcome varactor losses in tunable resonant elements with negative resistance circuitry has been shown feasible. Two-section passband filters were constructed with these elements using standard coupled resonator design considerations. The filters are small in size, light in weight, can be rapidly tuned over relatively wide frequency ranges, and have high-Q responses which are essentially free of spurious and harmonic passbands.

Acknowledgment

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Computer Optimized Multiple-Branch-Line Couplers

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Abstract—Computer aided design and optimization of microwave networks in the presence of discontinuities are presented. The discontinuity networks are evaluated using a planar waveguide model and are available as Fortran programs. The method is illustrated by the design of two and three branch line hybrids.

1. Introduction

A design approach is presented that yields computer optimized microwave networks in the presence of discontinuities such as bends, tee junctions, steps in impedance, etc., some of which are shown in Fig. 1.

The transmission line types considered are strip line, microstrip, and thin centered suspended strip line. A planar waveguide model is used to represent these structures (see Figs. 2 to 4), so as to simplify the derivation of the elements of the scattering matrix of the discontinuities. These transmission line types are widely used because they are light weight, economical, and readily reproducible using photographic methods. The computer analysis is then used as part of an optimization procedure to obtain locally optimum designs.

Since the computer aided design (CAD) technique is most easily illustrated by example, the design of a two-branch-line and a three-branch-line branch-line 3-dB coupler will be presented. A comparison between measured and computer predicted results of these couplers is included.

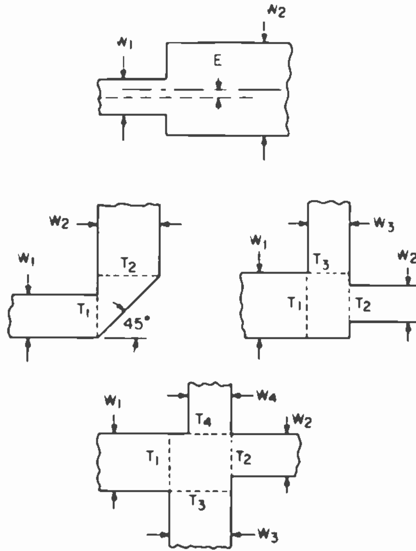


Fig. 1—Discontinuities in planar waveguide.

2. Planar Waveguide Model

The general method used to calculate the equivalent circuits of discontinuity structures requires the solution of complex integral equations. An approximate method of reduced mathematical complexity was originally proposed by Oliner for balanced strip line[1] and later refined by Wolf[2] to include microstrip. Whereas Oliner used Babinet equivalents to take advantage of existing solutions in waveguide, Wolf used a mode-matching technique to derive the discontinuity elements directly. The fundamental concepts of the method are given below.

When the ground plane spacing b, of Fig. 2 is much less than the wavelength in the dielectric, the electric and magnetic fields will be assumed constant along the y direction, i.e., normal to the conductors. The three dimensional structure is thus reduced to a two-dimensional or planar structure. To account for the fringing at the edges of the strip line, the width of the center conductor is increased and terminated in magnetic walls, as shown in Fig. 2. The strip line is bisected and represented as a waveguide of height $b/2$ and width W_{eff}, terminated in magnetic walls.[1] W_{eff} is given as

$$W_{eff} = b\frac{K(k)}{K(k')} + \frac{t}{\pi}[1 - \ln(2t/b)], \qquad [1]$$

where

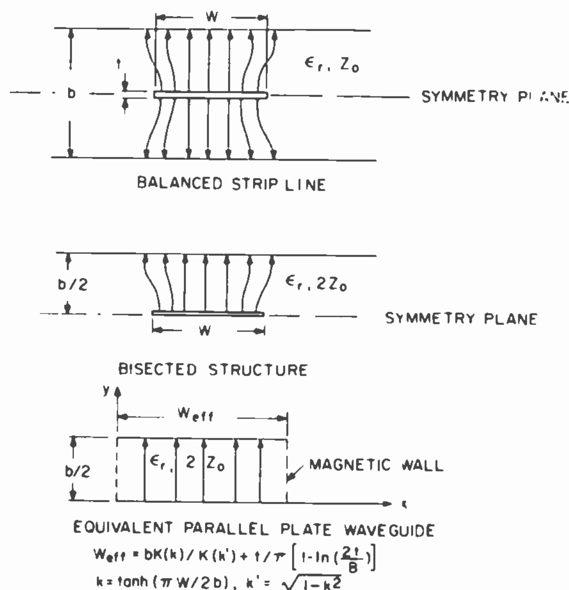


Fig. 2—Planar waveguide equivalent of balanced stripline.

$k = \tanh(\pi W/2b)$,
$k' = \sqrt{1-k^2}$,
t = thickness of center conductor,
W = width of center conductor,

and where $K(k)$ is the complete elliptic integral of the first kind of modulus k. When $W/b > 0.5$, W_{eff} can be approximated as

$$W_{eff} = W + \frac{2b}{\pi}\ln 2 + \frac{t}{\pi}\left[1 - \ln(2t/b)\right] \qquad [2]$$

The first term in Eq. [1] is the contribution to the effective width due to the fringe field of a zero-thick center conductor and the second term is a thickness correction. The steps in the transformation from stripline to the equivalent parallel-plate waveguide are summarized in Fig. 2. Because the stripline was bisected along the symmetry axis in the transformation to parallel-plate waveguide, the impedance of the dominant mode in the parallel-plate waveguide is twice the impedance of the stripline. As shown in Fig. 2 the dielectric medium ϵ_r is unaltered by the transformation. In addition to the TEM mode shown in Fig. 2, TE_{no} modes can also exist in the parallel-plate waveguide. These higher-order modes can be described by a scalar potential[2] ψ_{po} as

$$\psi_{po} = \sqrt{\frac{\epsilon_p}{W_{eff}b/2}}\sin\frac{p\pi x}{W_{eff}}, \quad \text{with } \epsilon_p = \begin{cases}1 \text{ for } p = 0\\ 2 \text{ for } p \neq 0\end{cases} \qquad [3]$$

The modal fields are derivable from Eq. [3] via a transverse gradient operation, i.e.,

$$\mathbf{e_p} = \mathbf{k} \times \nabla_t \psi_{po}$$

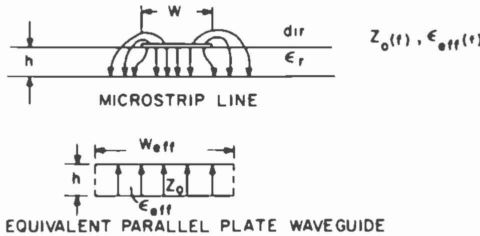
$$\mathbf{h_p} = \frac{\gamma}{j\omega\mu_0} \nabla_t \psi_{po} \qquad [4]$$

where $\mathbf{k}$ is unit vector in the z direction and γ the propagation constant:

$$\gamma = \left[\left(\frac{p\pi}{W_{eff}}\right)^2 - \omega^2 \epsilon_r \epsilon_0 \mu_0\right]^{1/2}. \qquad [5]$$

Having a complete set of modes allows the evaluation of planar discontinuities of the type shown in Fig. 1 by a mode matching technique as discussed in Ref. [2].

The transformation of the microstrip line to parallel-plate waveguide is shown in Fig. 3. Again it is assumed that the substrate thickness h is much less than a wavelength and variations normal to the conductors can be neglected. Because the microstrip line is composed of multiple dielectrics, the dominant mode is not pure TEM. This is reflected in a frequency dependent effective width, W_{eff}, and effective dielectric constant, ϵ_{eff}, for the equivalent parallel plate waveguide. Equations



$$W_{eff}(0) = \frac{h}{Z_0(0)} \sqrt{\frac{\mu_0}{\epsilon_{eff}(0)\epsilon_0}}$$ $\epsilon_{eff}(0)$ & $Z_0(0)$ GIVEN BY WHEELER

$$W_{eff}(f) = W + \frac{W_{eff}(0) - W}{1 + (f/f_p)^2}$$

$$f_p = \frac{c}{2 W_{eff}(0) \sqrt{\epsilon_{eff}(0)}}$$

$$\sqrt{\epsilon_{eff}(f)}^{\,*} = \frac{\sqrt{\epsilon_r} - \sqrt{\epsilon_{eff}(0)}}{1 + 4F^{-1.5}} + \sqrt{\epsilon_{eff}(0)}$$

$$F = \frac{4h}{\lambda_0}\sqrt{\epsilon_r - 1}\left[0.5 + \left\{1 + 2\ln\left(1 + \frac{W}{h}\right)\right\}^2\right]$$

* MOST RECENT DISPERSION RELATION BY YAMASHITA

Fig. 3—Planar waveguide equivalent of microstrip transmission line.

defining the effective width and the effective dielectric constant as a function of frequency are shown in Fig. 3. The most recent dispersion relation[3] is shown, as well as the most recent relation for $W_{eff}(f)$.[4] The scalar potential ψ_{po}, is frequency dependent through W_{eff} and is given by Eq. [3] with $b/2$ replaced by h, the substrate thickness. Similarly γ is given by Eq. [5] with ϵ_r replaced by ϵ_{eff}.

For the suspended substrate configuration shown in Fig. 4, it is assumed that the dielectric substrate thickness h is much less than the ground plane spacing b and that $b \ll \lambda$. These constraints imply an effective dielectric constant near unity with little dispersion and the validity of the planar model. Because of the complex geometry, the effective dielectric constant, ϵ_{eff}, and characteristic impedance, Z_o, of the suspended strip line must be determined by numerical methods[5] or measurements. The next step in the transformation to parallel-plate waveguide is to let the suspended substrate line be equivalent to a balanced stripline of dielectric constant ϵ_r equal to ϵ_{eff} and characteristic impedance Z_o. For thin substrates of low dielectric this has been found to be valid. The transformation from balanced stripline has already been described in Fig. 2.

Using the parallel-plate waveguide model for microstrip, Wolf et al[2] derived the scattering matrices of the junctions shown in Fig. 1. Using the relations shown in Fig. 2, the programs can be modified and used for balanced stripline or suspended stripline.

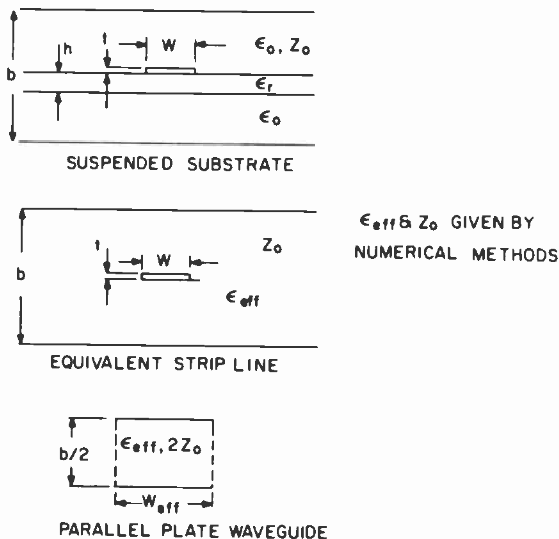


Fig. 4—Planar waveguide equivalent of suspended substrate transmission line.

3. Network Formulation of 3-dB Coupler

The 2-branch branch-line 3-dB coupler was modeled as a series of tee junctions connected by transmission lines, as shown in Fig. 5. The tee junctions are identical looking into the coupler ports and are described by scattering matrices from Wolf's programs for given w_0, w_1, and w_2. The input impedance corresponding to w_0 is 50 Ω and w_1, w_2, θ_1, and θ_2 must be determined so that the coupler will be optimized over a specified bandwidth centered at a prescribed frequency. The optimization will be discussed later.

Due to the high degree of symmetry of the coupler, even- and odd-mode bisection theorems were used to formulate the scattering matrix of the branch-line coupler.[6] The even- and odd-mode bisections reduce the four-port coupler network to two two-port networks, one associated with the even-mode bisection and one with the odd-mode bisection as shown in Fig. 6. The elements of the four-port scattering matrix, S_{ij}, are related to the two two-port scattering matrices as follows:

$$S_{11} = \frac{S_{11+} + S_{11-}}{2}, \quad S_{13} = \frac{S_{12+} + S_{12-}}{2}$$

$$S_{12} = \frac{S_{11+} - S_{11-}}{2}, \quad S_{14} = \frac{S_{12+} - S_{12-}}{2} \qquad [6]$$

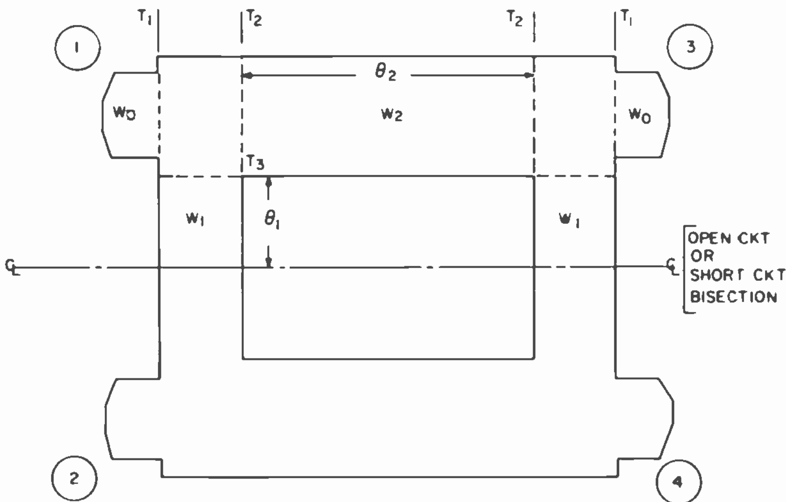


Fig. 5—Model for two-branch-line coupler optimization.

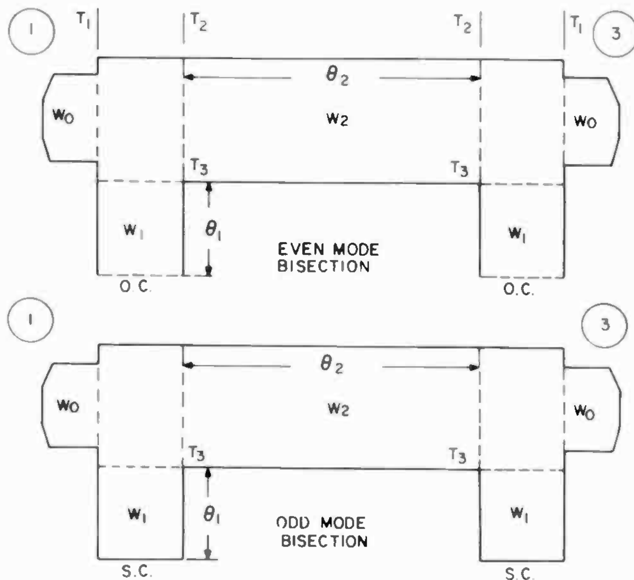


Fig. 6—Two-port characterization of branch-line coupler.

where

S_{11} = input reflection coefficient
S_{12} = isolation
S_{13} = straight through coupling
S_{14} = diagonal coupling

and where the subscripts + and − denote even- and odd-mode bisections, respectively. The elements $S_{ij\pm}$ are derived from the following considerations.

Knowing the scattering matrix of the tee junction $\tilde{R}$ derived from mode matching techniques at reference planes T_1, T_2, T_3, the open or short circuit termination at θ_1 from T_3 in the symmetry plane will reduce this 3×3 matrix to a 2×2 matrix. That is, at port 1 at reference planes T_1, T_2,

$$\tilde{S}'_{\pm(1)} = \begin{pmatrix} \left[R_{11} + \dfrac{R_{13}^2\Gamma}{1 - R_{33}\Gamma}\right] & \left[R_{12} + \dfrac{R_{13}R_{23}\Gamma}{1 - R_{33}\Gamma}\right] \\ \left[R_{12} + \dfrac{R_{13}R_{23}\Gamma}{1 - R_{33}\Gamma}\right] & \left[R_{22} + \dfrac{R_{23}^2\Gamma}{1 - R_{33}\Gamma}\right] \end{pmatrix} \quad [7]$$

where R_{ij} are the elements of the tee junction and

$\Gamma = \pm\, e^{-j2\theta_1}$.

Again, the + sign is for the even-mode bisection and the − sign is for the odd-mode bisection.

Similarly at port 3,

$$\tilde{S}'_{\pm(3)} = \begin{pmatrix} \left[R_{22} + \dfrac{R_{23}^2\Gamma}{1 - R_{33}\Gamma}\right] & \left[R_{12} + \dfrac{R_{13}R_{23}\Gamma}{1 - R_{33}\Gamma}\right] \\ \left[R_{12} + \dfrac{R_{13}R_{23}\Gamma}{1 - R_{33}\Gamma}\right] & \left[R_{11} + \dfrac{R_{13}^2\Gamma}{1 - R_{33}\Gamma}\right] \end{pmatrix} \quad [8]$$

In order to combine $\tilde{S}'_{\pm(1)}$ and $\tilde{S}'_{\pm(3)}$ to form $\tilde{S}_\pm$ for the two ports, $\tilde{S}'_{\pm(1)}$ is rotated through the electrical angle θ_2 via the following similarity transformation,[7]

$$\tilde{S}''_{\pm(1)} = \tilde{P}\tilde{S}'_{\pm(1)}\tilde{P}$$

where

$$\tilde{P} = \begin{pmatrix} 1 & 0 \\ 0 & e^{-j\theta_2} \end{pmatrix}.$$

Therefore

$$\tilde{S}''_{\pm(1)} = \begin{pmatrix} S'_{\pm(1)_{11}} & S'_{\pm(1)_{12}}e^{-j\theta_2} \\ S'_{\pm(1)_{12}}e^{-j\theta_2} & S'_{\pm(1)_{22}}e^{-j2\theta_2} \end{pmatrix} \quad [9]$$

where $S'_{\pm(1)_{ij}}$ are the elements of the scattering matrices $\tilde{S}'_{\pm(1)}$. Combining $\tilde{S}''_{\pm(1)}$ and $\tilde{S}'_{\pm(3)}$, the complete scattering matrices $\tilde{S}_\pm$ of the two ports are given as

$$\tilde{S}_\pm = \begin{matrix} \left[S''_{\pm(1)_{11}} + \dfrac{S''_{\pm(1)_{12}}{}^2 S'_{\pm(3)_{11}}}{1 - S''_{\pm(1)_{22}}S'_{\pm(3)_{11}}}\right] & \left[\dfrac{S''_{\pm(1)_{12}}S'_{\pm(3)_{12}}}{1 - S''_{\pm(1)_{22}}S'_{\pm(3)_{11}}}\right] \\ \left[\dfrac{S''_{\pm(1)_{12}}S'_{\pm(3)_{12}}}{1 - S''_{\pm(1)_{22}}S'_{\pm(3)_{11}}}\right] & \left[S'_{\pm(3)_{22}} + \dfrac{S'_{\pm(3)_{12}}{}^2 S''_{\pm(1)_{22}}}{1 - S''_{\pm(1)_{22}}S'_{\pm(3)_{11}}}\right] \end{matrix} \quad [10]$$

The scattering matrix of the coupler $\tilde{S}$ can now be constructed using Eqs. [6] through [10]. For convenience, we define $\Gamma_1 = e^{-j2\theta_1}$ and $\Gamma_2 = e^{-j2\theta_2}$. Then, from Eqs. [7] through [10],

$$S_{11_+} = R_{11} + \frac{R_{13}^2\Gamma_1}{1 - R_{33}\Gamma_1} + \frac{\left[R_{12} + \dfrac{R_{13}R_{23}\Gamma_1}{1 - R_{33}\Gamma_1}\right]^2 \left[R_{22} + \dfrac{R_{23}^2\Gamma_1}{1 - R_{33}\Gamma_1}\right]\Gamma_1}{1 - \left[R_{22} + \dfrac{R_{23}^2\Gamma_1}{1 - R_{33}\Gamma_1}\right]^2 \Gamma_2} \qquad [11a]$$

$$S_{11_-} = R_{11} - \frac{R_{13}\Gamma_1}{1 + R_{33}\Gamma_1} - \left[R_{12} \frac{R_{13}R_{23}\Gamma_1}{1 + R_{33}\Gamma_1}\right]^2 \left[R_{22} \frac{R_{23}^2\Gamma_1}{1 + R_{33}\Gamma_1}\right]\Gamma_1 \qquad [11(b)]$$

$$S_{12_+} = \frac{\left[R_{12} + \dfrac{R_{13}R_{23}\Gamma}{1 - R_{33}\Gamma_1}\right]^2 \Gamma_2}{1 - \left[R_{22} + \dfrac{R_{23}^2\Gamma_1}{1 - R_{33}\Gamma_1}\right]^2 \Gamma_2} \qquad [11(c)]$$

$$S_{12_-} = \frac{\left[R_{12} - \dfrac{R_{13}R_{23}\Gamma_1}{1 + R_{33}\Gamma_1}\right]^2 \Gamma_2}{1 - \left[R_{22} - \dfrac{R_{23}^2\Gamma_1}{1 + R_{33}\Gamma_1}\right]^2 \Gamma_2} \qquad [11(d)]$$

thus the scattering matrix of the coupler is completely determined.

To extend the bandwidth over which a branch line coupler will operate, additional branches are added. A three-branch branch-line coupler is shown in Fig. 7. As for the two-branch case, the hybrid is modeled as a series of tee junctions separated by lengths of transmission line. From Fig. 7 it is seen that the input tee junctions are identical, leaving the center tee section dissimilar. The scattering matrix of the 3-branch coupler is derived in the same way as the two-branch coupler, i.e., even and odd mode bisections are used to reduce the four port matrix to two two-port matrices. Eq. [6] is then used to determine the four-port scattering elements, as for the two-branch hybrid.

Let $\tilde{R}$ be the scattering matrix of the input tee junctions and $\tilde{T}$ be the scattering matrix of the center tee junction. Then the elements of $\tilde{S}_\pm$ are,

$$S_{11_+} = T''_{11} + \frac{T''^{2}_{12}\Gamma_2 \left[R_{22} + \dfrac{R_{23}^2\Gamma}{1 - R_{33}\Gamma_1}\right]}{1 - T''_{22}\left[R_{22} + \dfrac{R_{23}^2\Gamma_1}{1 - R_{33}\Gamma_1}\right]\Gamma_2} \qquad [12(a)]$$

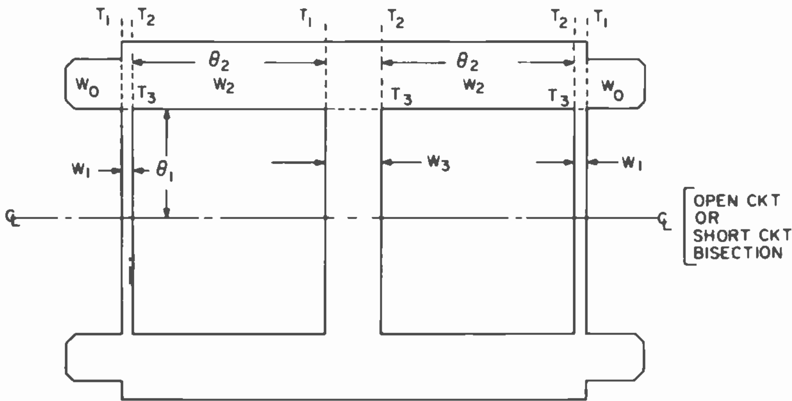


Fig. 7—Model for three-branch-line coupler optimization.

where

$$T''_{11} = R_{11} + \frac{R_{13}^2\Gamma_1}{1 - R_{33}\Gamma_1} + \frac{\left[R_{12} + \frac{R_{13}R_{23}\Gamma_1}{1 - R_{33}\Gamma_1}\right]^2 \left[T_{11} + \frac{T_{13}^2\Gamma_1}{1 - T_{33}\Gamma_1}\right]\Gamma_2}{1 + \left[R_{22} + \frac{R_{23}^2\Gamma_1}{1 - R_{33}\Gamma_1}\right]\left[T_{11} + \frac{T_{13}^2\Gamma_1}{1 - T_{33}\Gamma_1}\right]\Gamma_2} \qquad [12(b)]$$

$$T''_{12} = \frac{\left[R_{11} + \frac{R_{13}^2\Gamma_1}{1 - R_{33}\Gamma_1}\right]\left[T_{12} + \frac{T_{13}^2\Gamma_1}{1 - T_{33}\Gamma_1}\right]}{1 - \left[R_{22} + \frac{R_{23}^2\Gamma_1}{1 - R_{33}\Gamma_1}\right]\left[T_{11} + \frac{T_{13}^2\Gamma_1}{1 - T_{33}\Gamma_1}\right]} \qquad [12(c)]$$

$$T''_{22} = T_{11} + \frac{T_{13}^2\Gamma_1}{1 - T_{33}\Gamma_1} + \frac{\left[T_{12} + \frac{T_{13}^{2}{}^{2}\Gamma_1}{1 - T_{33}\Gamma_1}\right]^2 \left[R_{22} + \frac{R_{23}^2\Gamma_1}{1 - R_{33}\Gamma_1}\right]\Gamma_2}{1 - \left[R_{22} + \frac{R_{23}^2\Gamma_1}{1 - R_{33}\Gamma_1}\right]\left[T_{11} + \frac{T_{13}^2\Gamma_1}{1 - T_{33}\Gamma_1}\right]\Gamma_2} \qquad [12(d)]$$

$$S_{12+} = \frac{T''_{12}e^{-j\theta_2}S'_{12(3)}}{1 - T''_{22}\Gamma_2 S'_{11(3)}} \qquad [13]$$

where

$$S'_{12(3)} = R_{12} + \frac{R_{23}R_{13}\Gamma_1}{1 - R_{33}\Gamma_1}, \quad [13(a)]$$

$$S'_{11(3)} = R_{22} + \frac{R_{23}^2\Gamma_1}{1 - R_{33}\Gamma_1}. \quad [13(b)]$$

To obtain S_{11-} and S_{12-}, replace Γ_1 with $-\Gamma_1$ in Eqs. [12] and [13].

4. Optimization

Having achieved a computer analysis for deriving the S-parameters of various branchline hybrids, it becomes desirable to develop an optimization procedure. The four hybrid terms S_{11}, S_{12}, S_{13}, S_{14} can be combined algebraically to arrive at an objective function to be minimized. The primary characteristic of the objective function is that its value decreases for a corresponding improvement in the performance of the hybrid, and it has a minimum at the ideal operating point. There is no unique objective function for any one problem and the choice is based on experience. Ideally the objective function contour will be well-behaved, having no discontinuities and only one minimum. Under these conditions the global optimum can always be found. Unfortunately, these properties rarely hold in practice and the designer is forced to accept a local minimum based on his initial starting point. Indeed a global optimum can be "practically" guaranteed if a grid search in the vector space is performed, and then fined tuned from the best point generated in the search. This creates many practical problems regarding computer processing time and is infeasible in most applications involving more than a few variables, as is the case here.

For the branch-line hybrid an objective function, called U, is of the form

$$U(\chi) = \sum_{freq} f_1[(|S_{13}| - g_1)^2 + (|S_{14}| - g_2)^2] + f_2(|S_{11}|^2 + |S_{12}|^2) + f_3(|S_{13}| - |S_{14}|)^2, \quad [14]$$

where

χ is the input column vector corresponding to the physical dimensions of the hybrid of dimension n;

f_1, f_2, f_3 are the scalar weighting factors and are ≥ 0 (note: $f_3 = 0$ if $g_1 = g_2$);

g_1, g_2 are the scalar goals for the magnitude of the coupled ports S_{13} and S_{14} respectively; and

freq. is a set of frequencies near the center band of operation.

The factor f_1 weights the transmission as the deviation from the designed transmission goals squared, and the factor f_3 provides an additional correction factor for balancing the transmission ports provided that the goals are equal. The term weighted by f_2 provides an error term for isolation and input VSWR, which are equally weighted. This error function will evaluate to zero if the performance is exactly the desired performance at each frequency in the sum and to something greater than zero if there is any deviation.

There are two classes of optimization algorithms, direct-search and gradient methods. The direct-search method uses no derivative information and essentially reduces the objective function by trial and error, perhaps making use of pattern information that it can discover. The gradient methods employ derivative information in computing a direction of search and, in general, the objective function is evaluated along this direction to reach the minimum.[8] Of the gradient methods, Fletcher's algorithm is still considered to be one of the best when gradients are known,[9] and has initially been chosen for this application.[10] Since no analytical expressions exist for the gradients, they must be computed by numerical-differencing, a time consuming process. In light of this, the gradient method was initially chosen for the optimization procedure because good search directions can be found.

Fletcher's quasi-Newton method minimizes an objective function U of an input vector $\chi = [\chi_1, \chi_2, \ldots, \chi_n]^T$ where the T represents transpose, and is based on the second order Taylor series expansion.

$$U(\chi + \Delta\chi) = U(\chi) + (\nabla U)^T \Delta\chi + \tfrac{1}{2}(\Delta\chi)^T G \Delta\chi + \ldots \quad [15]$$

where

$$\nabla U = \begin{bmatrix} \dfrac{\partial U}{\partial \chi_1} \\ \vdots \\ \dfrac{\partial U}{\partial \chi_n} \end{bmatrix} \qquad G = \begin{bmatrix} \dfrac{\partial^2 U}{\partial \chi_1^2} & \cdots & \dfrac{\partial^2 U}{\partial \chi_1 \partial \chi_n} \\ \vdots & \ddots & \vdots \\ \dfrac{\partial^2 U}{\partial \chi_n \partial \chi_1} & \cdots & \dfrac{\partial^2 U}{\partial \chi_n^2} \end{bmatrix}$$

provided that ∇U and G exist, and G is termed the Hessian matrix. Now given a vector χ let the notation χ_k denote the kth iteration; the basic iteration to find χ_{k+1} (where $U(\chi_{k+1})$ is hopefully less than $U(\chi_k)$) is

$$\chi_{k+1} = \chi_k + \alpha_k P_k \quad [16]$$

where

$$P_k = -H_k \nabla U_k. \quad [17]$$

Here H_k is ideally chosen to be G^{-1} and this is based on assuming that $(\nabla U)^T \Delta \chi$ is small near the minimum point.

Needless to say, computing G and its inverse to find H_k would be a time consuming process and herein lies the main feature of Fletcher's method. Instead an updating formula is used to find H_{k+1} from H_k:

$$H_{k+1} = H_k + A_k + B_k \tag{18}$$

where

$$A_k = \frac{\Delta \chi_k \Delta \chi_k^T}{\Delta \chi_k^T (\nabla U_{k+1} - \nabla U_k)} \tag{19}$$

and

$$B_k = \frac{-H_k[\nabla U_{k+1} - \nabla U_k][\nabla U_{k+1} - \nabla U_k]^T H_k}{[\nabla U_{k+1} - \nabla U_k]^T H_k [\nabla U_{k+1} - \nabla U_k]}. \tag{20}$$

Fletcher proves that if H_k is positive definite them H_{k+1} given according to Eq. [18] is as well, thus proving convergance since H_o is defined in the algorithm to be positive definite, usually the unit matrix. Fletcher goes on to prove that H_k converges to G^{-1} for a quadratic function U.

The scalar α_k in Eq. [16] must also be chosen, ideally to minimize U along the direction P_k. In the final iterations when H_k is a very good approximation to G^{-1} and ∇U is approaching zero, a good choice for α_k is $\alpha_k = 1$. But in the first iterations when H_k is a poor approximation to G^{-1}, $\alpha_k = 1$ may not work well; so a quadratically good choice would be $\alpha_k = 2(U_{k+1} - U_k)/(\nabla U_k)^T P_k$. Further if the assumption is made that reduction on U_k to U_{k+1} is approximately the same as that for U_{k-1} to U_k, then the equation for α_k becomes

$$\alpha_k = \text{minimum of 1 and } 2(U_k - U_{k-1})/(\nabla U_k)^T P_k. \tag{21}$$

Provided $U_{k+1} < U_k$ and $|\nabla U(x_k + \alpha_k P_k)^T P_k| < -\rho \nabla U_k^T P_k$ then the α_k given above is used.[11] Whenever this criterion is not met, an extra function evaluation is necessary. Since a low accuracy line search is being performed $\rho = 0.9$ is used. If $\nabla U(\chi_k + \alpha_k P_k)^T P_k > 0$ then cubic interpolation is used to find α_k; if $\nabla U(\chi_k + \alpha_k P_k)^T P_k < 0$ than linear extrapolation is used to determine α_k.

Finally the stopping criteria for the optimization is that each element in $\chi_k - \chi_{k-1}$ be less than the corresponding element in ϵ where $\epsilon = (\epsilon_1, \epsilon_2, \ldots, \epsilon_n)^T$ and ϵ is termed the tolerance vector. The overall performance of Fletcher's algorithm is very good, requiring on the average of approximately 1.25 function evaluations per iteration.

The effects of the weighting terms in Eq. [14] can be seen in Figs. 8–10. The center frequency is 3.3 GHz and the set freq is {3.0, 3.15, 3.3, 3.45,

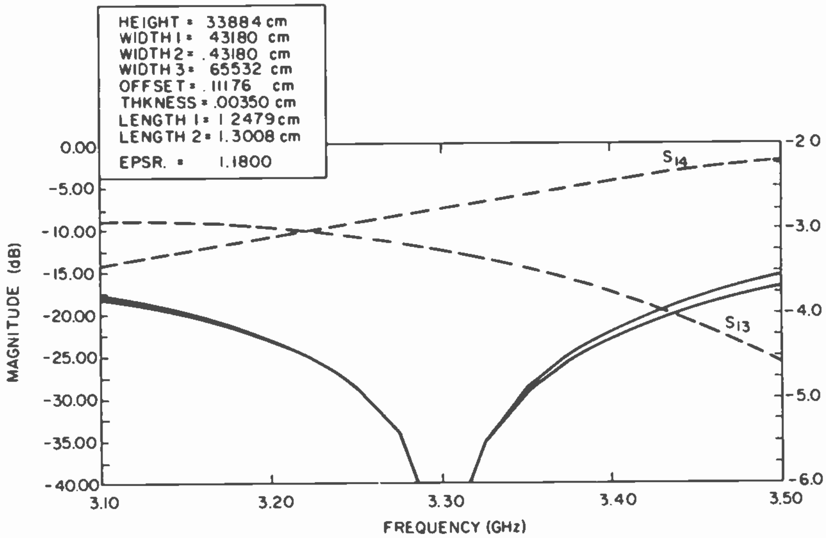


Fig. 8—Optimization of two-branch-line coupler (f_1, f_2, f_3) = (100, 500, 100).

3.6}. Fig. 8 shows the optimization of a single section hybrid with the weighting terms as $f_1 = 100, f_2 = 500, f_3 = 100$. This effectively emphasizes the design goal of low input VSWR and high isolation, but sacrifices the balance of transmission in the coupled arms. Fig. 9 is the optimization result from the same starting point but with $f_1 = 500, f_2 = 100, f_3 = 100$;

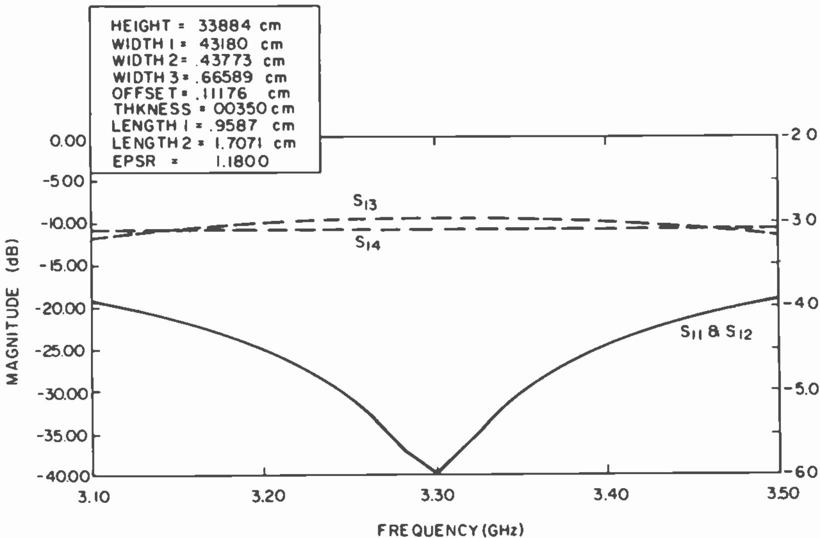


Fig. 9—Optimization of two-branch-line coupler (f_1, f_2, f_3) = (500, 100, 100).

here the center band isolation and input VSWR are not as good but a very good balance for the transmission is achieved. Finally, Fig. 10 shows the results, again from the same starting point as for the other two, but with $f_1 = f_2 = f_3 = 100$. Here the importance of weighting is clearly visible and the choice is up to the designer as to the relative importance of the design goals.

5. Comparison of Calculated and Measured Results of Two- and Three-Branch-Couplers

To check the validity of both the scattering matrix of the T-junctions and the optimization technique, two and three branch-couplers were fabricated. The effective dielectric constant for the suspended stripline shown in Fig. 11 was found experimentally[12] to be 1.18. The dielectric substrate is 8 mil Teflon fiberglass with 1 oz. Cu. The dielectric constant of the substrate is 2.55. To position the substrate and keep it from warping, a hexcell filler was used to sandwich the substrate as shown in Fig. 11. The effective dielectric constant of 1.18 includes the hexcell material.

The starting values for the two-branch coupler were 35 Ω and 90° for the straight thru line and 50 Ω and 90° for the shunt branch line. The line lengths are referenced center to center at 3.3 GHz. The impedance values are for a hybrid with a simple shunt junction. The optimization

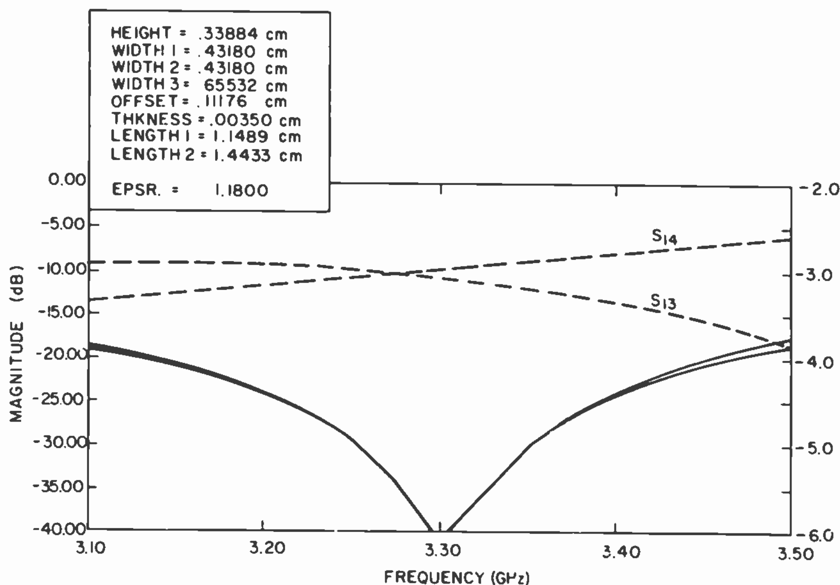


Fig. 10—Optimization of two-branch-line coupler (f_1, f_2, f_3) = (100, 100, 100).

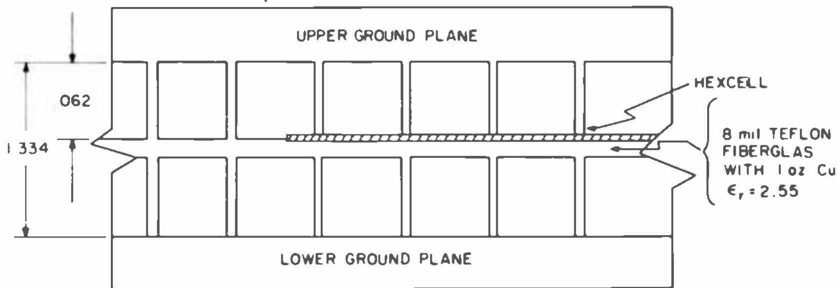


Fig. 11—Hybrid cross section.

routine essentially left all parameters constant except the length of the shunt branch line, which was increased to 114°, approximately a 27% increase. The conductor pattern is shown in Fig. 12 and a plot of the measured and computed results are shown in Fig. 13. If the power coupled to port (2) (isolation) is used as a reference, the measured response is shifted up in frequency by less than 2%. The coupling at 3.3 GHz is within 0.1 dB at the output ports with about 0.25 dB insertion loss. From Fig. 13 it is seen that the overall agreements between measured and calculated results is quite good. The VSWR is below 1.2:1 for most of the band as shown in Fig. 14.

The starting values for the three-branch coupler were as follows[13]: 50

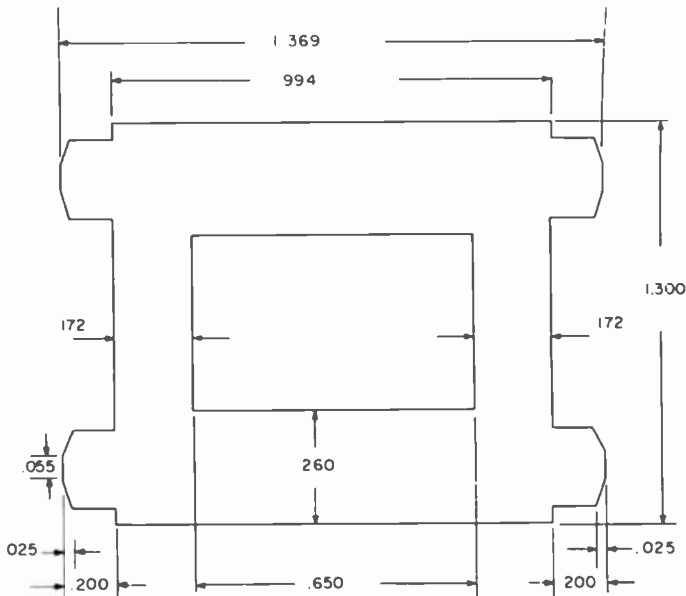


Fig. 12—Suspended stripline 3-dB coupler: f_0 = 3.3 GHz, material 8-mil Teflon fiberglass.

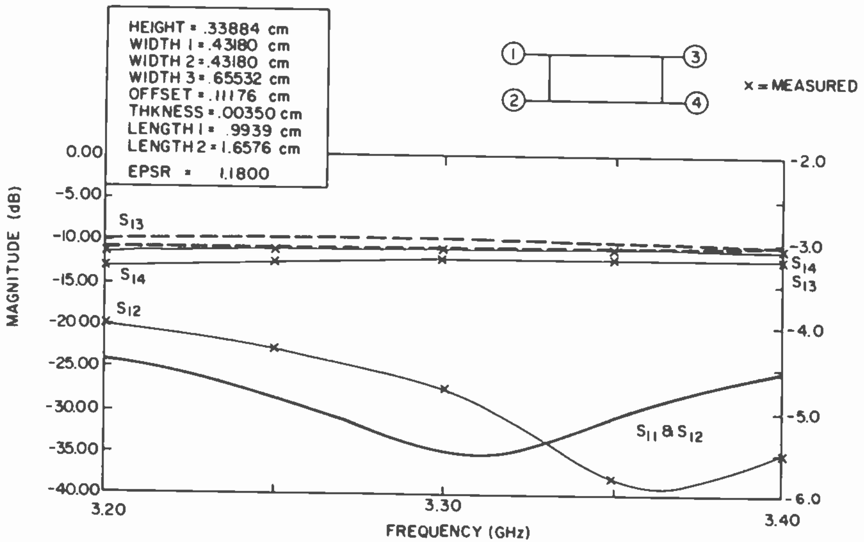


Fig. 13—Comparison of measured and calculated results for a 3-dB two-branch coupler.

Ω and 90° for the straight through lines, 121 Ω and 90° for outer branch lines, and 71 Ω and 90° for the central branch line. As for the two-branch hybrid, the line lengths are measured between centerlines at 3.3 GHz, and the starting impedance values neglect the reactive elements of the tee junctions. The optimized transmission lines are 40 Ω and 90°, 120 Ω and 107°, and 46 Ω and 107°, respectively. A sketch of the circuit pattern is shown in Fig. 15. Because of the high impedance line, the line widths were increased by 1.4 mils to compensate for the over etching during processing.

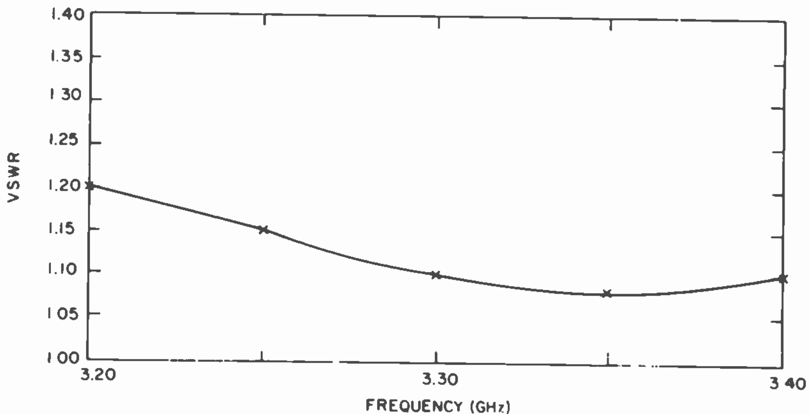


Fig. 14—Two-branch coupler VSWR.

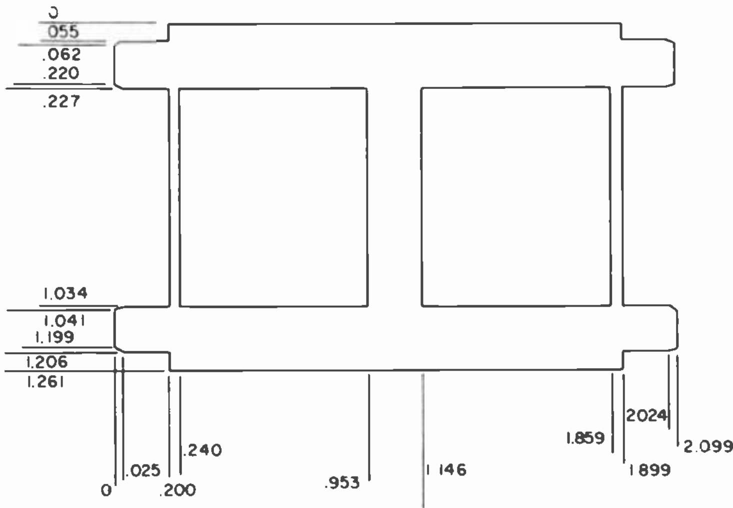


Fig. 15—Three-branch 3-dB coupler: f_0 = 3.3 GHz, material 8-mil Teflon fiberglass.

The measured and calculated straight-through coupling S_{13} in dB is shown in Fig. 18. As for the 2-branch hybrid, there appears to be a small shift upwards in frequency. The minimum isolation over the frequency band is 28 dB. The reduced isolation may be due in part to the imperfect terminations used during the measurement and in part to the SMA connectors. The hybrid is well matched over the frequency band, being less than 1.15:1 and 1.05:1 at 3.3 GHz as shown in Fig. 19. From the coupling values at 3.3 GHz as given in Fig. 16 to 19, the insertions loss was calculated to be less than 0.2 dB. This includes the connector loss.

6. Conclusions

The computer aided analysis and optimization procedures have been used successfully to design two actual circuits constructed in suspended substrate. Based on the good agreement between calculated and measured results, the mathematical model of planar networks appears valid and could be applied to other microwave component designs and general design lay-outs where the effects of discontinuities are of importance.

The analysis portion of the optimization routine is naturally suited to tolerance studies, where the effect of changing many parameters is desired.

In various experiments with the program, the optimization procedure always was able to reduce the objective function by orders of magnitude (provided of course that the initial point was not already an optimum).

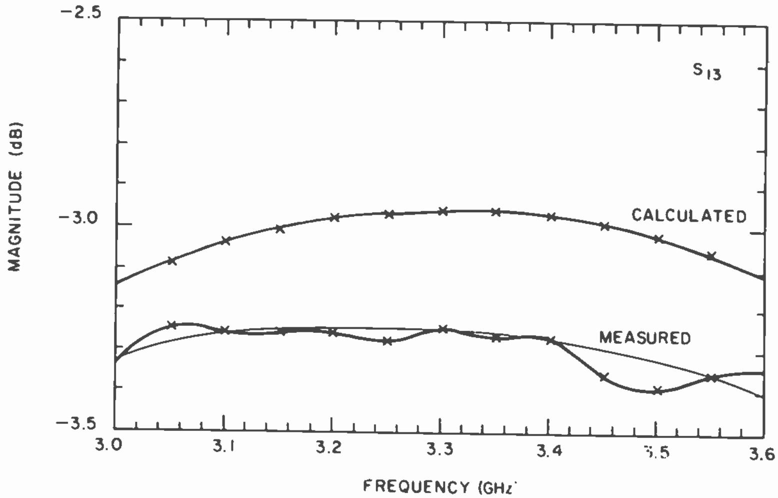


Fig. 16—Comparison of measured and calculated transmission for a three-branch coupler.

Also, various local minima were discovered by starting with different initial points, emphasizing the fact that the global minimum cannot be found easily. Even neglecting that the operating point found cannot be guaranteed to be the absolute ideal point, the optimization procedure does provide a better operating point, thus giving the designer a powerful tool when combined with good analysis.

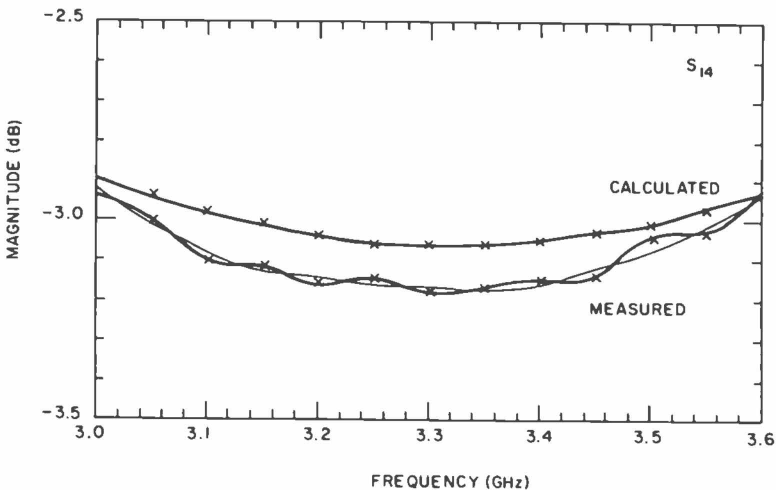


Fig. 17—Comparison of measured and calculated transmission for a three-branch coupler.

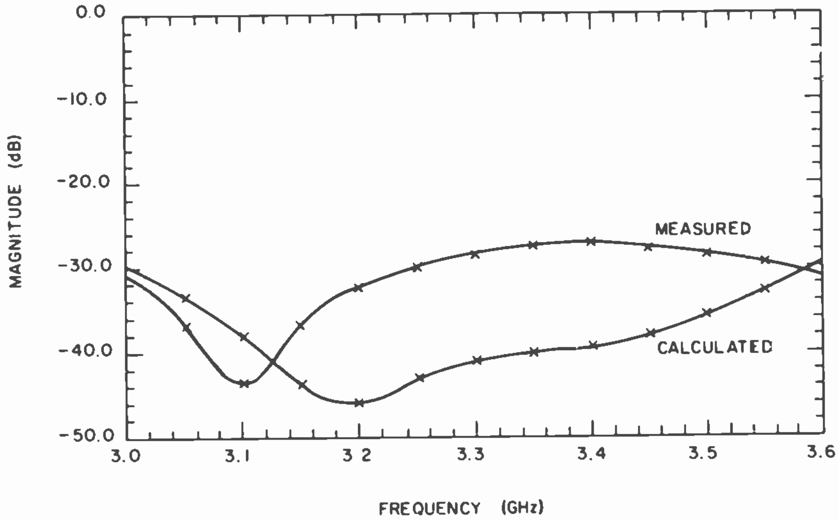


Fig. 18—Comparison of measured and calculataed isolation for a three-branch coupler.

Future work should include producing designs at higher frequencies to discover where the modelling and, hence, the analysis fails. Also, loss could be incorporated into the modelling, hopefully producing an even better simulation capability. Since the gradients of the objective function are not known analytically, perhaps switching to one of the direct search methods may provide a more efficient optimization procedure.

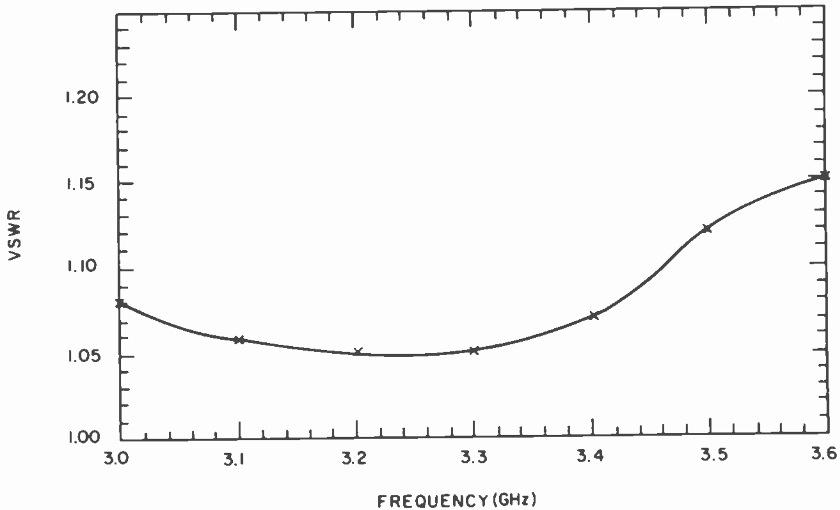


Fig. 19—VSWR of the three-branch coupler.

7. Acknowledgments

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Localized Hyperthermia Treatment of Cancer

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Abstract—Localized hyperthermia (sustained heating of tissues to temperatures of about 42–43.5°C) is one of a number of unconventional methods for treating cancer that are currently receiving increased attention from oncologists. This paper gives a brief review of the effects of hyperthermia on malignant cells and tissues and of methods for producing localized hyperthermia in animals and humans. Radiofrequency and microwave apparatus developed at RCA Laboratories for clinical applications of localized hyperthermia is described in some detail. Clinical results with a variety of cancers are encouraging.

Introduction

There are three major established methods for treating cancer: surgery, chemotherapy, and radiation therapy. In surgery one tries to cut out the cancer, in chemotherapy one tries to poison it with chemicals, and in radiation therapy one tries to kill it with ionizing radiation such as X-rays. Although impressive progress has been made and continues to be made in applying these three methods either alone or in combination, the 5-year relative survival rate for cancer patients* has improved little over the past 30 years. In the U.S. the 5-year relative survival rate is

* The 5-year relative survival rate is the probability of a person remaining alive 5 years after having been diagnosed as having cancer, the rate being adjusted for the probability of death from other causes. The actual 5-year cancer survival rate (i.e., the rate that is not adjusted for the probability of death from other causes) is currently about 33% in the U.S. Both rates exclude skin cancers other than melanoma (melanoma is a highly dangerous form of skin cancer that is derived from cells containing pigments), and carcinoma diagnosed in situ (i.e., diagnosed before the cancer has become invasive). See reference 1 for a detailed discussion of survival rates.

currently estimated to be about 41%, only about two percentage points better than it was in 1950. These statistics, as well as similar statistics on cancer mortality trends, indicate that surgery, chemotherapy, and radiation therapy are beginning to assume the characteristics of mature technologies: advances tend to be evolutionary rather than revolutionary, substantial improvements (e.g., increasing the relative survival rates by a few percentage points) take a very long time and require high investments, etc. It is for these reasons that a small but growing number of oncologists are taking a serious look at nonconventional methods for treating cancer. Prominent among these nonconventional methods is hyperthermia where one tries to destroy cancers with the help of heat.

The use of heat in the treatment of cancer is very old, in fact considerably older than either chemotherapy or radiation therapy. The first scientific paper on the effect of high temperature on cancer is generally credited to a German physician, W. Busch,[2] who described in 1866 the disappearance of a soft tissue sarcoma* following a high fever in a patient with erysipelas. Between 1866 and the end of the 19th century, a number of other reports on spontaneous remission of cancers in patients who had episodes of high fever appeared in the literature, and some physicians reported on successfully treating cancer patients by artifically inducing fever with bacterial toxins.[3] After radiation therapy was introduced at the turn of the century, good clinical results were also reported when heating was combined with radiation therapy.** Following this pioneering work on fever therapy, toxin therapy, and combined hyperthermia-radiation therapy, the exploitation of the anti-tumor properties of heat proceeded at a relatively slow pace for several decades, although much basic scientific work was done on the effects of heat on malignant cell cultures and animal tumors, and there were occasional papers reporting encouraging clinical results with hyperthermia. During the past decade, however, the pace of work on hyperthermia has picked up considerably, and there are now groups in many parts of the world working on hyperthermia research and patient treatment.

The present paper deals with one form of hyperthermia treatment of cancer, namely localized hyperthermia (as opposed to whole-body hyperthermia). The paper is organized into five parts: general background on cancer, the effect of hyperthermia on malignant cell cultures and on

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* A sarcoma is a malignant tumor of connective tissues, such as fat, muscle, bone, etc.

** One of the physicians working on combined hyperthermia-radiation therapy wrote in 1915: "If I may venture a prediction, it is this: that the treatment of cancer, by low degrees of heat, to be followed in the advanced cases with massive doses of x-ray delivered through the medium of the Coolidge tube, is to prove, as soon as its merits are understood and appreciated, the greatest advance so far reached in the treatment of early and late cancer." [4]

animal and human cancers, methods for inducing localized hyperthermia with emphasis on the rf and microwave apparatus developed at RCA Laboratories, clinical results obtained with localized hyperthermia, and conclusions and outlook for the future.

What Is Cancer?

Cancer or malignant neoplasm can be defined as a relatively autonomous growth of tissue. The term "relatively autonomous" is used to indicate that the rate of growth of a cancer is to a large extent not controlled by the host organism but rather by the cancer itself. Cancers have the ability to metastasize, i.e., they can establish secondary growth in the host at

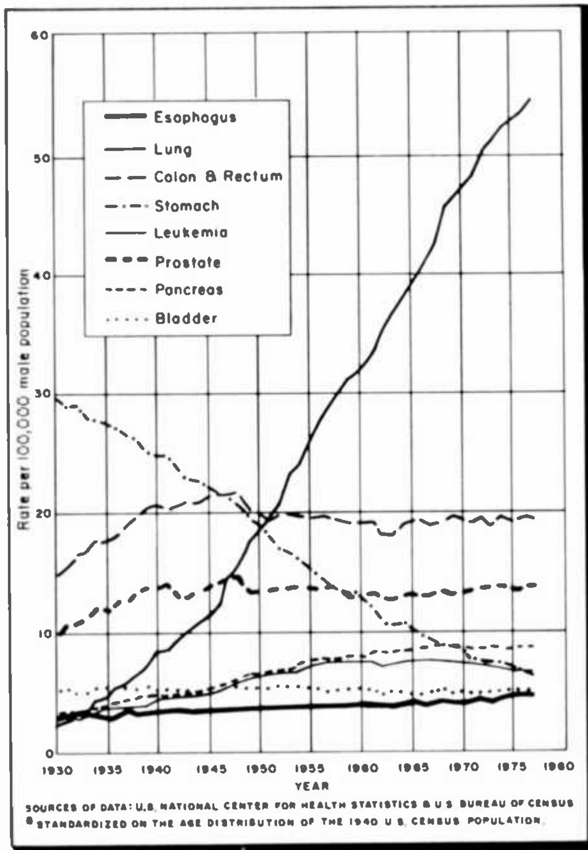

Fig. 1(a)—Age-adjusted cancer death rates for selected sites in males in the United States, 1930–1977.

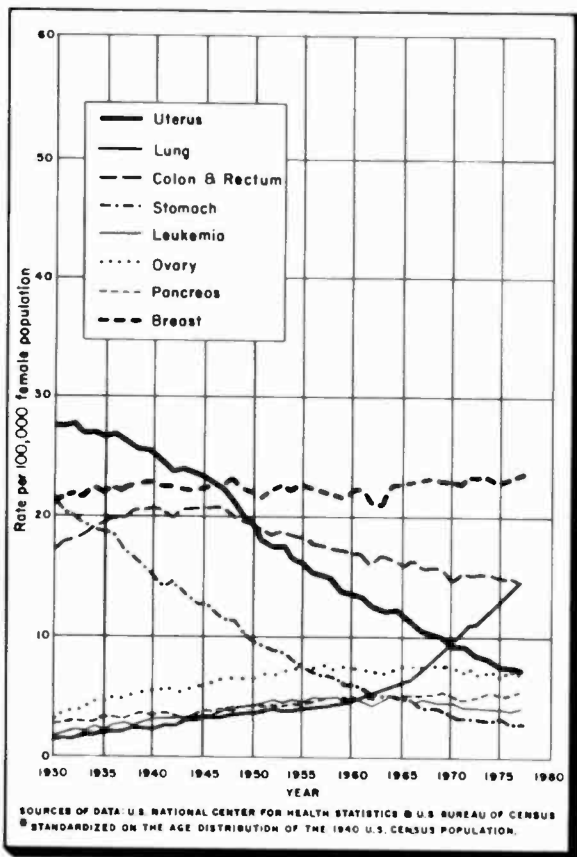

Fig. 1(b)—Age-adjusted cancer death rates for selected sites in females in the United States, 1930–1977.

locations distant from the original or primary tumor. There are various routes through which cancer cells can be carried to new locations, the most common being the blood circulation and the lymphatic system.

In humans, 75% of all cancers start in only 10 anatomic sites (this excludes cancer of the skin, which is the most common but also, except for melanoma, the most curable form of human cancer). These sites are colon and rectum, breast, lung and bronchus, prostate, uterus, lymph organs, bladder, stomach, blood and pancreas. Figs. 1(a) and 1(b) show the age-adjusted death rates from 1930–1977 for cancer at most of these sites in males and females in the United States.

Overall, cancer currently accounts for about 20% of all deaths in the U.S. During 1981, approximately 400,000 persons, or about 180 persons

per 100,000 population, will die of cancer in the U.S., making cancer the second most common cause of death in the U.S. (diseases of the heart are the leading causes).

Why Is Hyperthermia Effective In Treating Cancer?

The simple answer to the question posed in the heading of this section is that many malignant tumors are more sensitive to heat than normal tissues, and that one can often selectively heat tumors to higher temperatures than surrounding healthy tissues. It is therefore often possible to selectively destroy cancers either by heat alone or by a combination of heat and radiation therapy or chemotherapy. A more complete answer is that there appear to be a variety of complex interrelated factors involved in the action of hyperthermia against cancer. These factors range from effects at the cellular level to effects caused by the sluggish blood flow common in large tumors. The biological phenomena underlying many of these factors are at the present only poorly understood.

(a) Thermal Effects in Cell Cultures

Cultures of malignant cells grown in vitro (i.e., grown in an artificial medium rather than in a living organism) are often more sensitive to heat than are cultures of similar, but normal cells. This differential heat sensitivity is usually most pronounced when the temperature of the cultures is maintained at about 43°C for at least one hour. At temperatures below about 40°C, neither the malignant nor the normal cells are

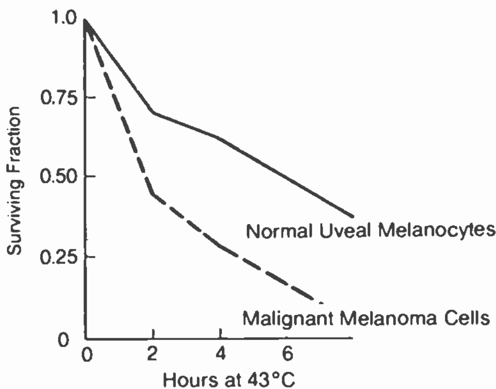

Fig. 2—Plot of surviving fraction of cells in vitro as a function of time for normal and for malignant melanoma cells. The cell cultures were maintained at 43°C. After Ref. [5].

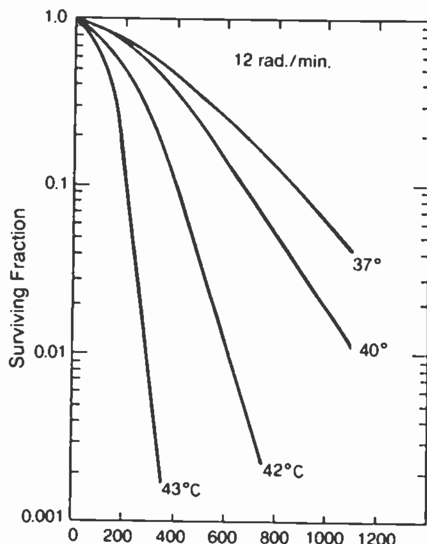

Fig. 3—Plot of surviving fraction of cells in vitro as a function of ionizing radiation dose for four different temperatures. After Ref. [5].

much affected by the heating, while at temperatures much above 45°C both types of cells are rapidly killed by the heat. A typical result obtained at 43°C for normal and malignant cells of the same type is shown in Fig. 2. Note that there is indeed a substantial difference in the surviving fractions between the two types of cells.

Studies of in vitro cell cultures also show that heat can increase the lethal effects of ionizing radiation and of certain chemotherapeutic agents. This is illustrated for the case of ionizing radiation in Fig. 3 which is a plot of surviving fraction for malignant cells in vitro as a function of radiation dose in rads.* The figure shows that for a dose of about 350 rads there is nearly a thousandfold increase in the lethal effect of the ionizing radiation when the temperature of the culture is increased from 37°C (98.6°F) which is normal body temperature to 43°C (109.4°F).

What are the reasons for the dramatic increase in the lethal effects of ionizing radiation when cell cultures are heated to about 43°C? There are no definitive answers yet, but the following two effects that have been observed in experiments with cell cultures offer important clues:

- Hyperthermia (i.e., sustained heating to about 42–43.5°C) appears to interfere with the repair of radiation-induced sublethal damage in cells.

* The rad is the unit of absorbed ionizing radiation dose (1 rad = 100 ergs/gm of absorbing material).

- Cells in the middle-to-late S-phase of the cell cycle* are most sensitive to hyperthermia. This happens to be the part of the cell cycle where cells are most resistant to damage by ionizing radiation. Thus the two modalities are complementary in their ability to damage cells. During the part of the cell cycle where ionizing radiation is most effective, hyperthermia is relatively ineffective, and vice versa.

Two other important thermal effects that have been observed in cell cultures need to be mentioned. First, hypoxic cells (i.e., cells that are poorly oxygenated) are more sensitive to hyperthermia than well oxygenated cells. The significance of this observation to clinical treatment will become clear in the next subsection. Second, some malignant cell cultures develop a thermal tolerance to hyperthermia after having been exposed to sublethal hyperthermic doses. This suggests that tumors should be raised to hyperthermic temperatures as rapidly as can be tolerated by the patient.

(b) Thermal Effects in Tumors

The destructive effect of heat on malignant as well as on healthy tissues is a function of the temperature to which the tissues are raised, and the length of time the tissues are maintained at the temperature. This is illustrated in Fig. 4 which is based on in vivo (i.e., in living organisms) experiments with a particular mouse tumor. The figure shows three ranges of combinations of temperature and time. In the upper range (A) most healthy and malignant tissues are destroyed. In the intermediate range (B) most healthy tissues survive, but the tumor is eradicated with no subsequent regrowth. (This is the range of most interest for therapeutic use.) In the lowest range (C) there is little or no damage to healthy tissue, but the damage to the malignant tissues is insufficient for the complete destruction of the tumor and the prevention of its regrowth.

The differential heat sensitivity of malignant versus healthy tissues illustrated in Fig. 4 does not appear to be primarily due to any intrinsic cellular effects of the type shown in Fig. 2. Rather, effects at the tissue level, particularly those associated with the vascular system of malignancies, appear to play a major role. Malignant tumors commandeer blood supplies from adjacent healthy tissues, and distribute this blood to their own tissues by means of their own vascular system. The exact nature of the tumor vascular system depends on the tumor type or even on the particular tumor itself. In general though, tumor vascular systems, particularly those of larger tumors, are not as efficient in moving blood

* When cells divide they usually proceed through a characteristic cycle which consists of distinct phases designated as G1, S, G2, M and D. In the S-phase DNA is synthesized.

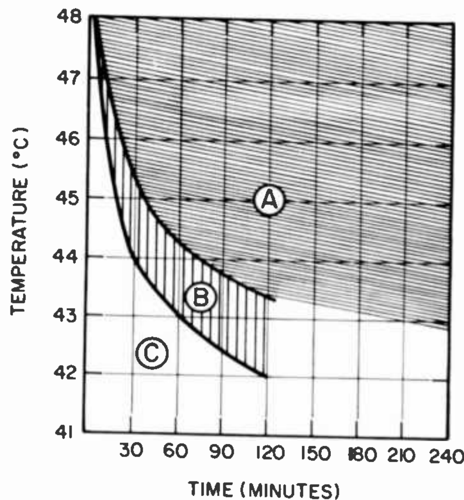

Fig. 4—Example of the effect of various temperature–time combinations on healthy versus malignant in vivo tissues. Range A: both healthy and malignant tissues are destroyed; range B: most healthy tissue survives, tumor is killed with no subsequent regrowth; range C: little or no damage to healthy tissue, tumor survives and regrows. After Ref. [5].

as are typical normal vascular systems. Moreover, while the blood flow in most normal tissues increases as the temperature of the tissues is increased from normal body core temperature (~37°C) to hyperthermic temperatures (~43°C),* the blood flow in many malignant tissues decreases with temperature above about 39°C and prolonged exposure to hyperthermic temperatures often causes irreversible damage to the tumor capillaries.**

Impaired blood flow in tumors causes reduced blood supply to malignant tissues. This reduced blood supply in turn causes high extracellular pH in the malignant tissue, a factor known to enhance thermal injury. Furthermore, the low blood flow deprives the malignant cells of nutrients, and nutrient deficient cells are particularly heat sensitive.

The impaired blood flow typical of many large tumors helps to make it often possible to selectively heat tumors to substantially higher temperatures than adjacent healthy, well vascularized tissues. When tissues are heated with localized hyperthermia, most of the heat is carried away from the heated tissues by the blood flow. As a result, for the same con-

* For example, in healthy human skin the local blood flow increases by almost a factor of ten when the temperature is raised from 37°C to 43°C.

** When tumors are treated with both ionizing radiation and hyperthermia, tumor blood flow is further reduced because the ionizing radiation damages the tumor vascular system.

Table 1—Approximate Useful Depth for Hyperthermia Treatments with Single Radiating Applicator

Frequency (MHz)	Depth (cm)	
	H	L
30	10	>20
100	5	>20
1000	3	15
2500	2	10
5000	1	5

H = Tumor shielded from applicator by tissues with high water content such as skin and muscle.
L = Tumor shielded from applicator by tissues with low water content such as fat and bone.

stant heat input the temperature of tumors with impaired blood flow will reach equilibrium at a higher temperature than will well vascularized normal tissues. If the localized hyperthermia is produced with radiofrequencies or microwaves, the differences between equilibrium temperatures of tumors and healthy tissues are often further increased, because there is typically about 50% more heating of tumor tissues (except for necrotic tissues) than of normal tissues for the same radiofrequency or microwave fields.[6] This is because tumor tissues usually have a significantly higher water content than do normal tissues, and radiofrequencies and microwaves are absorbed at a faster rate in tissues with high water content than in tissues with low water content (see Table 1).

Measurements on patients show that the differences in equilibrium temperature between tumors and healthy tissues when both are heated with rf or microwave radiation of the same power density can be as high as several degrees centigrade, a difference of important biological significance (see Figs. 3 and 4). Fig. 5 shows temperature-versus-time curves typical of cutaneous and subcutaneous tumors and of healthy tissues that are heated with microwaves. The curves were taken on a patient with an anaplastic neck tumor. The dotted curve is the surface temperature of the tumor as a function of time when the tumor was heated with the waveguide applicator of Fig. 9(a) with 1 W of 2450 MHz microwave power. Note that the tumor temperature stabilized at about 41°C. The solid curve is the skin-temperature-versus-time of healthy tissue on the contralateral side of the neck when heated the same way as the tumor. In this case the temperature stabilized at a value only slightly higher than 39°C. Similar results are often obtained when tumors are heated with radio frequencies. For example, when a subcutaneous melanoma in the groin of a patient was heated with 100 MHz radiation, the equilibrium tumor temperature was approximately 2°C higher than the temperature of surrounding normal tissues. In this instance, the temperatures of both

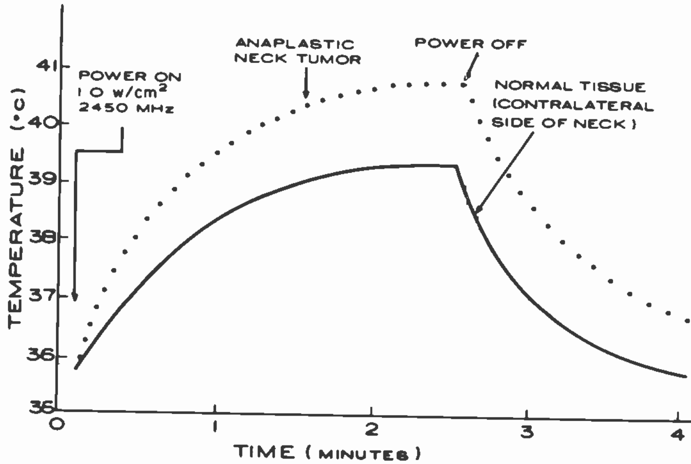

Fig. 5—Heating and cooling curves measured on a patient with an anaplastic neck tumor. Temperatures were measured with thermocouples placed at the center of the heated areas of the surface of the tumor and the surface of the contralateral side of the neck.

the tumor and the normal tissues were measured with a radiometer operating at 2450 ± 100 MHz. Such a radiometer noninvasively measures average tissue temperatures to a depth of approximately ½ cm.

The synergism between ionizing radiation and hyperthermia that was illustrated in Fig. 2 for in vitro cell experiments also exists at the tissue level, and in fact forms the basis of much of the present use of hyperthermia in treating cancer patients. Fig. 6 illustrates this synergism for the case of a mouse tumor that responded only partially to hyperthermia

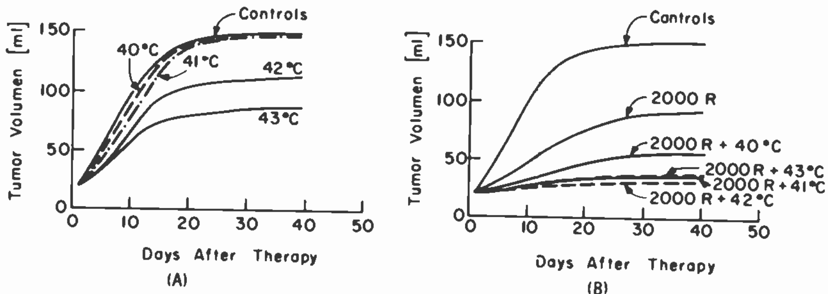

Fig. 6—Tumor volume versus days after treatment: (A) shows data for control animals and animals treated at four different temperatures with hyperthermia; (B) shows data for control animals and animals treated with 2000 rads of ionizing radiation with and without the addition of hyperthermia at four different temperatures. After Ref. [5].

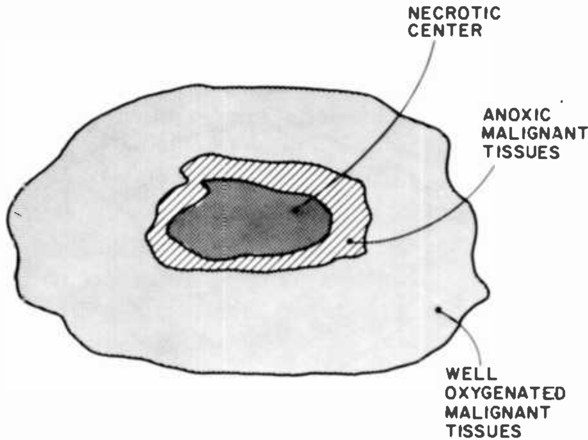

Fig. 7—Structure of a typical large tumor showing necrotic, poorly oxygenated, and well oxygenated tissues.

alone (Fig. 6a) or to radiation alone (two top curves of Fig. 6b). However, when the two modalities were combined (lower four curves of Fig. 6b), excellent response was obtained.

One of the reasons for the synergism between ionizing radiation and hyperthermia can be explained with the aid of Fig. 7 which shows the morphology of a typical large tumor. The periphery of the tumor draws its blood supply from the neighboring healthy tissue, and its tissues are well oxygenated. The center of the tumor is necrotic (dead) because the tumor vascular system failed to supply tissues in the center with sufficient nutrients to keep them alive. Between these two regions is a layer of malignant tissue that is anoxic (poorly oxygenated) but alive. These anoxic tissues are difficult to kill with ionizing radiation, since 2.5 to 3 times greater doses of ionizing radiation are necessary to kill hypoxic cells than to kill fully oxygenated cells. As a consequence, tumors that are treated only with ionizing radiation often shrink (malignant tissues in the well oxygenated outer layer are killed), but the tumors often regrow after some time because too many malignant hypoxic cells survived the radiation therapy. Hyperthermia complements radiation therapy because, as mentioned above, hypoxic cells are more sensitive to heat than are well oxygenated cells. This effect is often enhanced in practice because anoxic tissues due to their poor blood circulation can often be heated to substantially higher temperatures than are tissues with good blood circulation (e.g., because of the effects illustrated by Fig. 5).

A number of investigators have demonstrated synergism between chemotherapy and hyperthermia when treating animal and human

malignancies. The hyperthermia enhances the cytotoxicity (cell-poisoning ability) of several important chemotherapeutic drugs because some of these drugs become more active at higher temperatures. Also, blood vessels and cell membranes in tumors allow easier penetration of drugs when heated and, as was pointed out above, hypoxic tumor cells, which tend to be resistant to chemotherapeutic drugs, are especially sensitive to hyperthermia.

A particularly intriguing feature of localized hyperthermia is that one sometimes observes anti-cancer action at a distance from the treated area. For example, it has been shown that when one of a bilateral (on both sides) pair of human colonic cancers growing in the cheek pouches of hamsters is treated with localized hyperthermia, the growth of the untreated contralateral tumor is inhibited. Similar effects are sometimes seen in patients treated with localized hyperthermia; untreated lesions at distant sites occasionally regress or change from being radiation resistant to radiation sensitive. It has also been observed that metastases of certain tumors are less common in patients who are treated with localized hyperthermia followed, after some time interval, by surgery than are metastases in patients who are treated only with surgery.

A possible explanation of these "action-at-a-distance" phenomena is that localized hyperthermia stimulates the immune response of the host, thus strengthening the ability of the host to fight cancer throughout his entire body. Indeed, it has been shown by direct microscopic observations that localized hyperthermia helps to activate some of the "policemen" of the immune system (macrophages and T lymphocytes) causing them to infiltrate tumor sites. Another observation in support of the immunological theory is that the ability of localized hyperthermia to reduce or eliminate untreated metastatic lesions in animals is negated if the immunologic response of the animal is artificially repressed.

Methods for Producing Localized Hyperthermia

There are several methods currently in use for producing localized hyperthermia in cancer patients. The bases for these methods are either perfusion with externally heated blood, or direct heating of tissues with either ultrasound, radiofrequencies (rf), or microwaves.

In perfusion, blood is taken continuously from the patient, is heated, and is then reintroduced into the patient. Perfusion requires surgery (blood vessels of the patient must be connected to an external pump and heater). Also, because of the relatively poor blood circulation characteristic of many tumors, perfusion tends to heat healthy tissues faster than malignant tissues, which is a therapeutic disadvantage. However, if limbs of patients are perfused, large doses of chemotherapeutic agents

can usually be safely added to the circulating blood, since these agents will only be circulated in the limbs and will not reach the vital organs. This approach has been used with good results to treat melanoma on the limbs. Perfusion has also been used successfully to produce whole-body hyperthermia.

Ultrasound is useful for localized treatment of cutaneous and certain deep-seated tumors. It is easy to produce well-focused beams with relatively small apertures, since the wavelength of ultrasound in tissues is small. At a frequency of 1 MHz, for example, the wavelength in tissues is typically of the order of 1.5 mm. There is relatively little heating in fat as compared with muscle, which is usually an advantage in heating deep-seated tumors. Among the method's limitations are that large reflections from interfaces between various tissue types may result in hot spots from standing waves, the energy transfer from tissue to air is very poor (it is difficult to heat lungs), and there is very high absorption in bones.

Various methods have been devised to heat tumors with rf. In one method, the tumor to be heated is encircled by a number of implanted metallic needle-shaped electrodes, and rf voltages are applied across electrodes on opposite sides of the tumor. This causes rf currents to flow through the tumor and heat it. While well-localized heating can be produced with this method in many tumor sites, the method has the disadvantage of being invasive. Another rf method heats with rf currents that flow between capacitive electrodes held against the surface of the body of the patient. This method is well suited for localized heating of protruding tumors. However, when deep-seated tumors are heated with capacitive electrodes, the heating patterns inside the body of the patient are often difficult to predict. Also, excessive heating of skin and fat is often a problem unless multiple electrode configurations are used.

Localized and regional hyperthermia can also be produced by inductively inducing rf current flow in the tissues to be heated. Flat, pancake-shaped coils are useful for local heating of tumors near the surface of the body. Regional hyperthermia can be induced by encircling part of the patient's body with one or more coils. However, in regional hyperthermia produced this way the heating generally decreases toward the center of the body.

At RCA Laboratories, we have developed apparatus for producing localized hyperthermia in cancer patients based on yet another method, namely the use of antennas or applicators to broadcast rf or microwave energy into the tissues to be heated. The rf or microwaves travel through the tissues of the body in the form of exponentially-decaying waves, giving up energy to the tissues (dielectric heating) as they traverse them.

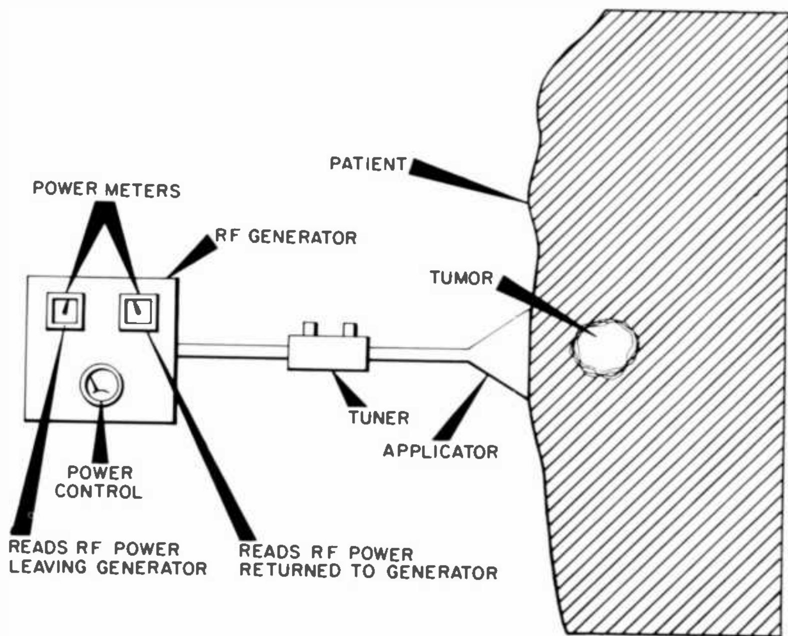

Fig. 8—Block diagram of typical hyperthermia system.

Fig. 8 is a block diagram of the apparatus used to induce localized hyperthermia with radiated rf or microwaves. Power produced by a generator is matched by means of a tuner into an applicator that radiates the power toward the tumor to be treated. Two power meters are provided, one for measuring the power leaving the generator, and a second for measuring the power reflected back to the generator. The depth to which the rf or microwaves that are radiated by the aplicator can penetrate into the patient and heat the tumor is primarily a function of the dielectric properties of the tissues shielding the tumor from the appli-

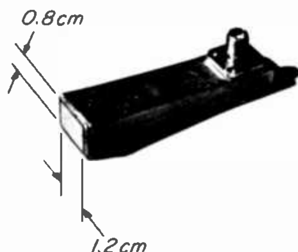

Fig. 9(a)—Microwave hyperthermia applicator (2450 MHz) filled with solid dielectric (used for treating small superficial lesions).

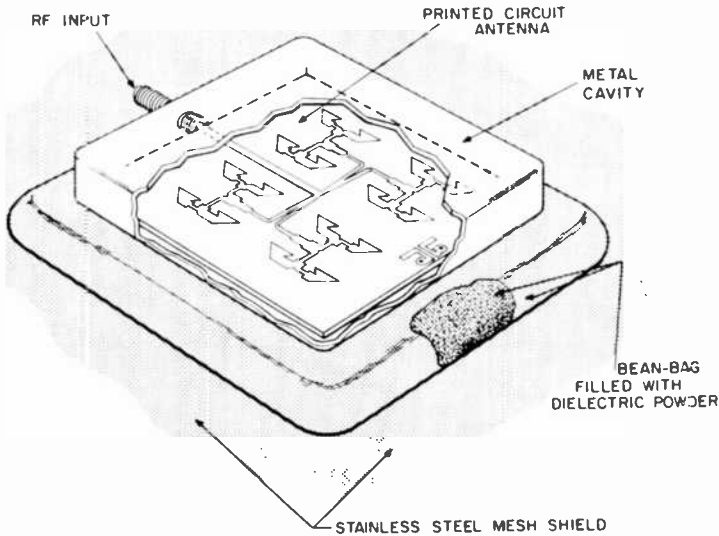

Fig. 9(b)—Microwave hyperthermia applicator (2450 MHz) using printed circuit antenna (for treating large superficial lesions and breast tumors).

cator and of the rf or microwave frequencies used. In general, the lower the water content of the shielding tissues, the deeper a wave at a given frequency can penetrate. Waves penetrate much deeper into fat (low water content) than into muscle (high water content). Also, at the frequencies of interest, the lower the frequency, the deeper the depth of penetration into tissues with a given water content. The approximate useful depths for localized hyperthermia treatments using a single radiating applicator are listed in Table 1.

Figs. 9(a)–(d) show four hyperthermia applicators that were developed at the Microwave Technology Center.[7–10] The applicators shown in Figs. 9a–9c operate at a microwave frequency (2450 MHz), the applicator of Fig. 9d operates at a relatively low rf frequency (27 MHZ).* With the microwave applicators it is possible to accurately focus the microwave energy into the tumors to be treated, but their use is limited to treating cutaneous and subcutaneous tumors, tumors located within or in the vacinity of natural body cavities, and tumors located in the breasts. The rf applicator can be used to treat deep seated tumors, but focusing is relatively poor (the wavelengths in tissues at 27 MHz are greater than

* 2450 MHz and 27.12 MHz are among frequencies set aside by the Federal Communications Commission for Industrial, Scientific and Medical applications. We have also built applicators that operate at 100 MHz, 300 MHz, 915 MHz, and 5800 MHz.

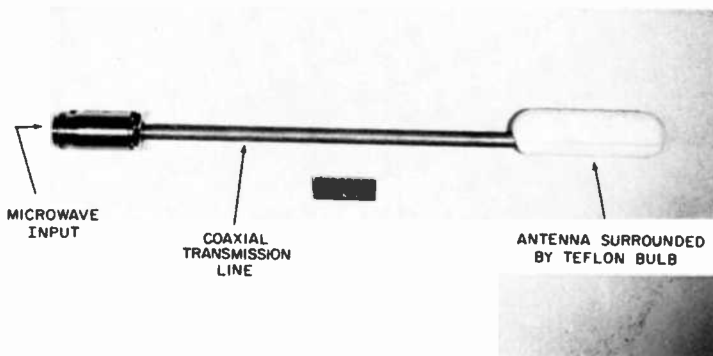

Fig. 9(c)—Coaxial microwave applicator (2450 MHz) (rectal applicator for treating prostate cancer).

1 meter). The rf or microwave power levels required to raise tissues to hyperthermic temperature range from about 1 W for the applicator of Fig. 9a to several hundred watts for the applicator of Fig. 9d.

All hyperthermia apparatus developed by us is first tried out on animals before any use on humans is attempted. The first study on animals carried out with our apparatus involved a group of 72 C3H mice.[7] Breast cancer (mammary adenocarcinoma) was induced by implants in all 72 mice: 54 animals received 4 hyperthermia treatments localized to the tumor site (43°C, 45 min., every other day) with the applicator of Fig. 9a, while 18 served as nontreated controls. Complete eradication of tu-

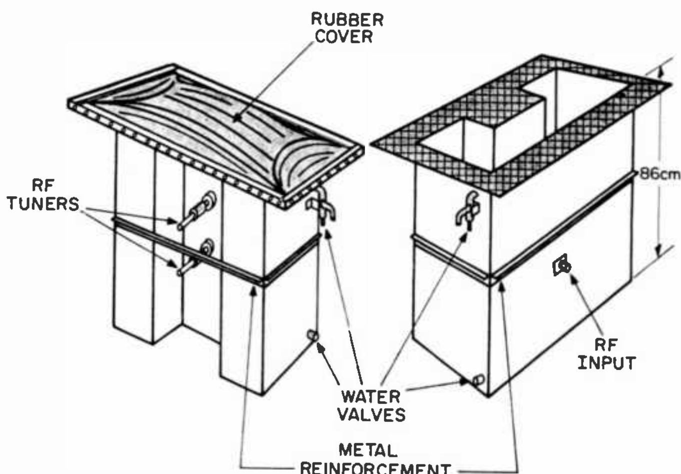

Fig. 9(d)—RF waveguide applicator (27 MHz) filled with deionized water (used for treating deep-seated tumors).

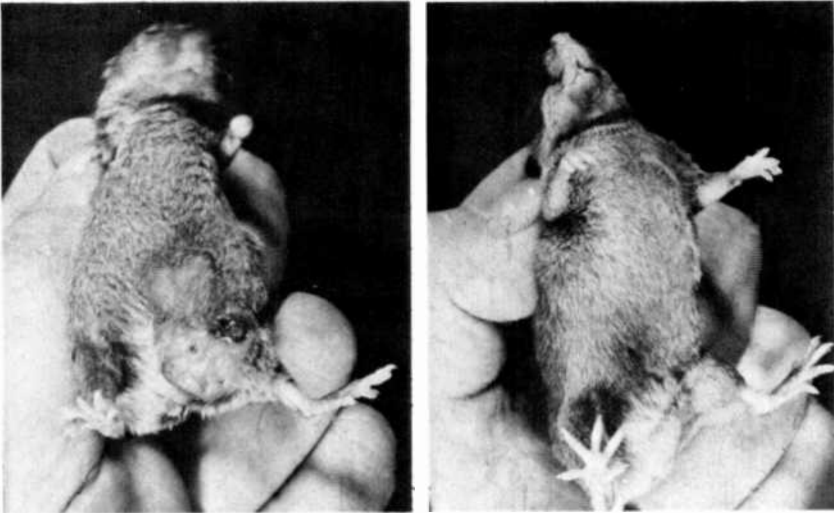

Fig. 10—Photographs of C3H mice used to study the effects of localized hyperthermia on mouse breast cancer: (a) control mouse with breast tumor; (b) mouse treated with localized hyperthermia.

mors was achieved in all the treated animals and they showed no evidence of tumor recurrence over an observation period of 4 months, whereas all 18 controls died within 4 weeks post-inoculation. Fig. 10a shows a control mouse with breast tumor; Fig. 10b shows a mouse treated with hyperthermia.

We usually use large animals, such as dogs and pigs, to measure the temperature distributions produced by our applicators. For example, Fig. 11 shows temperature versus time curves measured in the buttock of a 35-kg anesthetized pig that was heated with the 250 watts of 27 MHz power transmitted via the water-filled ridge waveguide applicator of Fig. 9d.[10] The skin of the buttock was maintained at 20°C by means of a water-cooled pad. The temperature in the buttock muscles was measured at depths of 2, 5, 7, and 9 cm by means of thermocouples. Note that after 20 minutes of heating the temperature distribution in the buttock is fairly uniform with the highest temperature occurring at a depth of 5 cm.

Fig. 12 is a photograph of a clinical setup for treating cutaneous or subcutaneous tumors using the applicator of Fig. 9b. The bean-bag of the applicator rests on the patient above the tumor that is to be treated with microwave power. Three thermocouples are placed underneath the bean-bag, one in contact with the surface of the tumor and two in contact with the surface of the healthy tissues surrounding the tumor. The

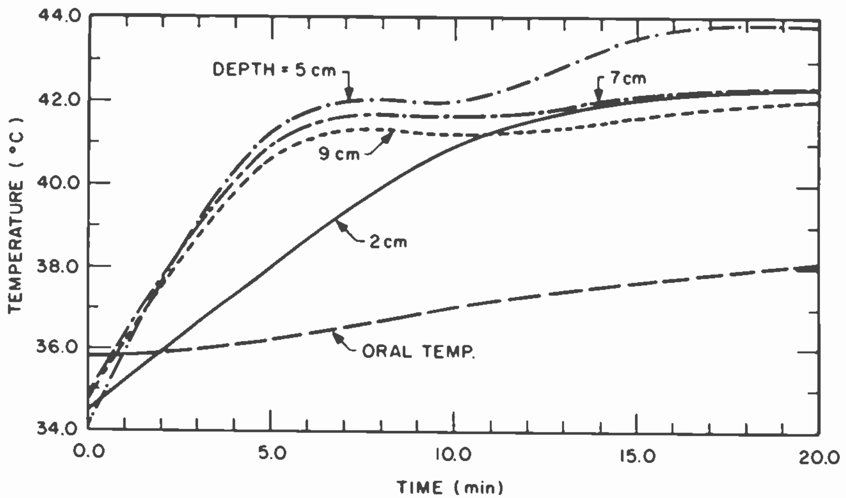

Fig. 11—Curves of temperature versus time measured in the buttock of an anesthetized pig. Also shown is the measured oral temperature of the animal.

output of the thermocouples is displayed in degrees Celsius on the thermocouple meter. The technician treating the patient stays with the patient during the entire treatment. He continuously monitors the

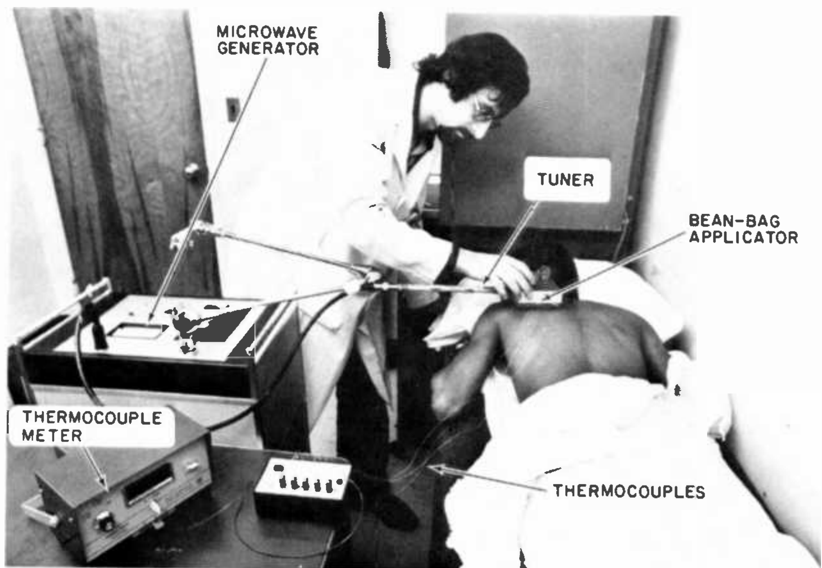

Fig. 12—Photograph of a clinical setup using the applicator of Fig. 9b. The photograph was taken at the Montefiore Medical Center, Bronx, N.Y.

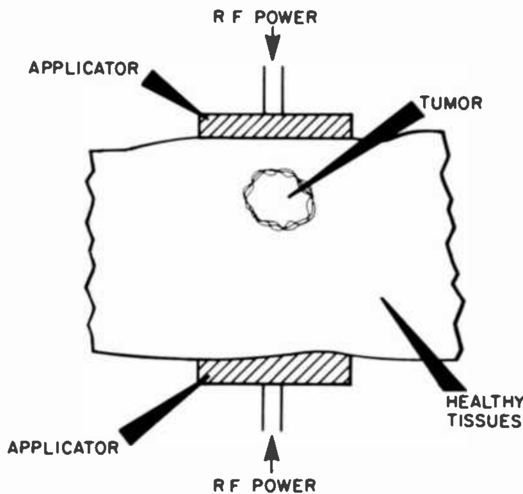

Fig. 13—Cross-fire arrangement for heating tumors with two applicators.

temperature of the tissues being heated and will immediately reduce the microwave power should the temperature of these tissues become dangerously high.

Deep seated tumors are often best heated with two or more applicators whose radiation patterns intersect at the tumor (also called "cross-fire" arrangement). This is illustrated in Fig. 13 for the case of two applicators facing each other. Cross-fire arrangements have proven useful for treating primary breast tumors. Here the breast is placed between two opposing bean-bag applicators of the type shown in Fig. 9b. Another important use of cross-fire arrangements is for treating deep-seated tumors located in the trunk of the body. Fig. 14 shows such an arrangement using two opposing 27 MHz water-filled ridged waveguide applicators.

Figs. 15 and 16 are photographs of a clinical setup for heating deep-seated tumors with two 27 MHz water-filled ridge waveguide applicators placed at right angles to one another. As can be seen from Fig. 15, each applicator is covered with a rubber bag filled with deionized water, a cooling pad, and a rubber bag filled with saline solution. The bags filled with deionized water are designed to prevent excessive local surface heating by spreading the high electric fields present at the edge of the applicators without attenuating the 27 MHz radiation emanating from the center of the applicator. (Deionized water is nearly lossless at 27 MHz.) The cooling pads cool the healthy tissues located between the deep-seated tumor and the applicator. They also cool some of the blood

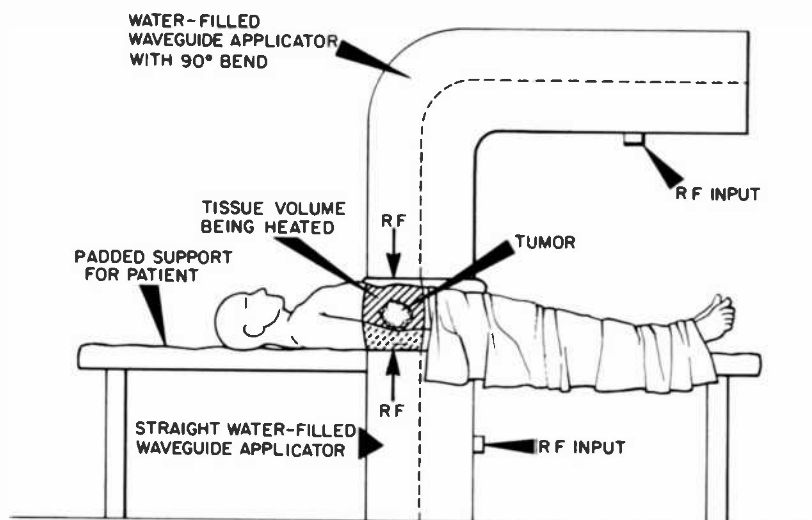

Fig. 14—Arrangement for producing localized hyperthermia in patient using two opposing water-filled waveguide applicators.

that enters the tumor and the adjacent healthy tissues. Since, as was pointed out above, the circulation in many tumors is poorer than in the healthy tissues that surround them, the cooled blood is usually more effective in cooling the healthy tissues than the malignant tissues. This makes it easier to heat tumors to hyperthermic temperature while keeping the temperatures of the healthy tissues at safe levels. The bags filled with saline solution are designed to further protect the healthy tissues of the patient. The 27 MHz radiation from the applicator passes through a rectangular cutout in the bags into the tissues directly above the tumor, while most stray radiation is absorbed by the saline solution. (Saline solution is a good absorber of 27 MHz radiation.) Fig. 16 shows a patient with carcinoma of the prostate being treated with the two 27 MHz applicators. The patient sits on one applicator, while the second applicator is against his lower back.

Clinical Results

Clinical experience in the United States with localized hyperthermia has been limited to date to a few hundred patients. All major types of cancers have been treated with localized hyperthermia including lung cancer, breast cancer, cancer of the colon, prostate cancer, head and neck cancer, skin cancers, etc. Fairly typical of the results obtained so far are the following statistics from Jefferson University in Philadelphia, Pa.,

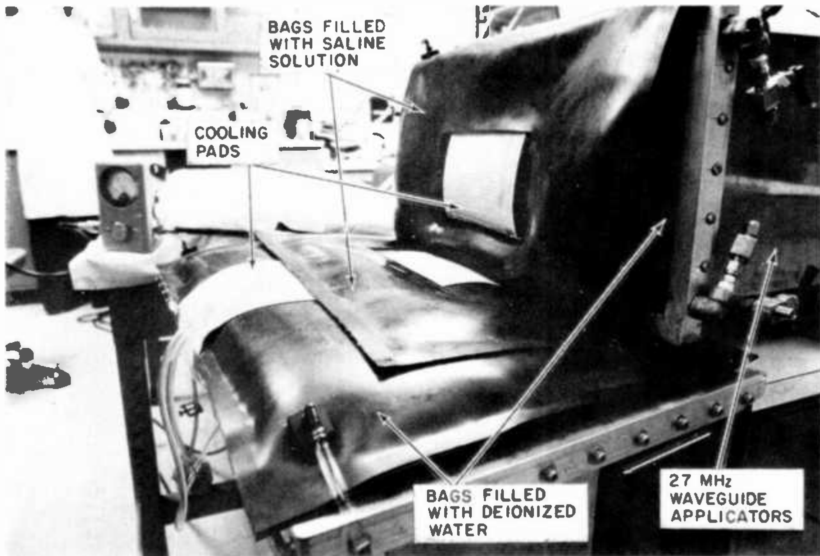

Fig. 15—Photograph of clinical setup using two 27-MHz water-filled ridged waveguide applicators placed at right angles to one another. The photograph was taken at the Montefiore Medical Center, Bronx, N.Y.

and Montefiore Medical Center in Bronx, N.Y., which cover a variety of tumors.* Using reduced amounts of ionizing radiation together with localized rf and microwave hyperthermia resulted in total regression of about one-third of all tumors treated, with biopsies showing no histological evidence of any viable remaining tumor. Another one-third of the tumors regressed partially (>50%), and about one-third showed no response. Statistics from hospitals that treated only cutaneous tumors with ionizing radiation and rf or microwave localized hyperthermia are better: 80% complete response (Memorial Hospital, New York City) and 56% complete response, 28% partial response (Hershey Medical Center, Hershey, Pa.).

While rf and microwave localized hyperthermia combined with reduced amounts of ionizing radiation has yielded encouraging results with many different types of malignancies, this type of therapy has been found to be particularly useful for treating breast cancers that have metastasized to the chest wall, tumors that regrow after having received close

* The basis for the selection of most patients for localized hyperthermia treatment at Montefiore Medical Center is currently as follows: (1) histologically proven malignancy; (2) failure or inapplicability of other therapeutic measures, i.e., tumor inoperable, operable but surgery refused, chemotherapeutic options exhausted, tumor radioresistant, or recurrence in previously irradiated area; (3) observable or measurable tumors; (4) ability to heat tumor mass with existing equipment (radiotherapy is added if previous radiotherapy did not exceed normal tissue tolerance).

Fig. 16—Photograph of patient with prostate tumor being treated with the setup of Fig. 12. The photograph was taken at the Montefiore Medical Center, Bronx, N.Y.

to the maximum tolerable dose of ionizing radiation, head and neck cancers, and certain malignant melanomas. Encouraging results have also been recently obtained with the applicator of Fig. 9c with 25 patients with prostate cancer at the Weizmann Institute of Science and the Kaplan Hospital in Rehovot, Israel, and with similar patients at Montefiore.

Patients who are candidates for hyperthermia treatment and their families and friends usually ask many questions about the treatments and their possible side effects. Following are some of the more commonly-asked questions, and answers to them.

Q. What is a typical treatment plan for a patient undergoing localized hyperthermia using rf or microwave radiators?

A. A minimum of about six to a maximum of about twenty hyperthermia sessions at the rate of 2 to 3 sessions per week. Each session lasts about 45 minuts to one hour. During each session, the temperature of the tumor or tumors to be treated is gradually raised to the hyperthermic range (~42–43.5°C), and is maintained in this temperature range for the remainder of the session. Ionizing radiation treatments are given either before or after the hyperthermia sessions.

Q. Are localized rf or microwave hyperthermia treatments painful?

A. Most patients tolerate localized hyperthermia treatments well, and feel comfortable during the treatments. Some patients, however, feel pain when the temperature of the treated area is raised for the first time to the hyperthermic range. In such patients, the technicians administering the hyperthermia treatment will reduce the temperatures of the treated areas to values that feel comfortable to the patients. The technicians will then gradually increase the temperatures, always staying below the threshold of pain of the patients. Eventually, even the most sensitive patients get used to the heating and learn to tolerate hyperthermic temperatures.

Q. Can localized hyperthermia treatments be given on an outpatient basis?

A. Yes. In fact, most of the patients being treated with the RCA-developed equipment are outpatients.

Q. Does localized rf or microwave hyperthermia produce side effects in or near the treated area?

A. When carefully applied, there are at most minor regional side-effects associated with localized hyperthermia. Some patients develop skin blisters or superficial ulcerations on the treated areas, and in some cases there is subcutaneous fibrosis (replacement of normal tissue by fibrous tissue), but in general most healthy tissues tolerate hyperthermic temperatures well. In fact, some surface tumors heal so well after hyperthermia treatments that it is difficult to tell where the tumors had originally been located. (Healthy tissues can, of course, be damaged by heat, particularly if they are heated to temperatures above the hyperthermic range. It is therefore of great importance that localized hyperthermia treatments be given only by well-trained technicians who are supervised by physicians familiar with the thermal tolerance limits of various tissues and organs.)

Q. Does localized hyperthermia produce any systemic side effects?

A. The tissues that are destroyed by localized hyperthermia are usually removed from the tumor sites by the blood circulation and the resulting waste products in the blood are removed by the kidneys. The kidneys of the patient may become overloaded if too much tumor tissue is destroyed too quickly by the localized hyperthermia.

Q. Can localized hyperthermia treatments promote distant metastases?

A. There are no indications at the present time that localized hyperthermia treatments do in any way promote the occurrence of

distant metastases. However, it will take many more years of careful recordkeeping and analysis before one can be absolutely certain of this. In the meantime, it is probably useful, as a precaution, to (1) accompany the hyperthermia treatments by at least a small dose of radiation, and (2) be as certain as possible that the tumor temperature does get raised to the hyperthermic range.

Conclusions and Outlook for the Future

Localized hyperthermia has several features that make it an attractive modality for treating malignant tumors. The most important of these features are (a) the relative safety of localized hyperthermia compared to conventional methods of treating tumors, (b) the selective destructive effect of heat above a threshold level of about 42.5°C on malignant versus normal tissues, (c) the ability to selectively heat many tumors to substantially higher temperatures than adjacent healthy tissues, particularly if the heating is done with rf or microwaves, (d) the sensitizing effect of heat when used in conjunction with ionizing radiation therapy, leading to reduced radiation doses and increased therapeutic ratios, (e) the apparent stimulation of immune processes by hyperthermia leading to increased host defenses against tumor growth, and (f) the sensitizing effects of hyperthermia when used in conjunction with chemotherapy.

A convenient way to produce localized hyperthermia is to use rf or microwave radiation. A variety of cutaneous, subcutaneous, and deep seated tumors have been safely treated with this method. Therapeutic results have been encouraging. In particular, a number of tumors that did not respond to conventional therapies responded well to combinations of localized hyperthrmia and reduced amounts of radiation therapy.

The number of cancer patients that are being treated with localized hyperthermia is likely to rapidly increase during the next few years. A growing number of oncologists are becoming familiar with the therapeutic possibilities of localized hyperthermia, and the equipments for producing localized hyperthermia are constantly being improved. Much emphasis will probably be placed on overcoming the present main limitation of localized hyperthermia, namely that one presently treats only local manifestations of cancer (i.e., particular tumors), rather than the systemic aspects of the disease. Promising approaches to treating the whole body of the patient include combining localized or regional hyperthermia with immunotherapy, chemotherapy, or tumor acidification,[11] scanning the whole body of the patient sequentially with regional hyperthermia, or whole-body hyperthermia.

Acknowledgments

The apparatus for producing localized hyperthermia with rf and microwave radiation described in this paper was developed over a period of several years in a cooperative program between the Radiotherapy Department of the Montefiore Medical Center and the Microwave Technology Center of the RCA Laboratories. The author wishes to express his deep appreciation to his colleagues on this program: Dr. Charles Botstein, Dr. Esther Friedenthal, Dr. Jozef Mendecki, and Steve Weber of Montefiore and Elvira Beck, Markus Nowogrodzki, Robert Paglione, and Frank Wozniak of RCA Laboratories, and also to the many patients who had the courage to participate in the initial clinical trials. The author also wishes to thank William Hittinger, Dr. Kerns Power and Dr. William Webster for their continuing encouragement of this work.

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Solid-State Antenna Switching

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Abstract—Solid state antenna switching on sophisticated exterior communication systems can replace mechanically driven rotary switches with improved performance parameters. Within the exterior communications system range of 10 KHz to 400 MHz, PIN diodes and conventional P-N junction diodes along with associated control and monitor functions are employed. Mechanical override backup is also provided to ensure minimum system "down time" in the event of a diode failure. P-N junction diodes are used for receive frequencies of 10 to 300 KHz. Long carrier lifetime PIN diodes are used for transmit/receive frequencies from 2 to 30 MHz with a power handling capability of 1,000 watts cw. PIN diodes utilizing micro strip technology are used for receive/transmit frequencies of 225 to 400 MHz with a power handling capability of 100 watts cw.

1. Introduction

Very Low Frequency (10–500 KHz), High Frequency (2–30 MHz) and Ultra High Frequency (225–400 MHz) computer controlled antenna switching is presently achieved with electro-mechanical, multideck, rotary-wafer switches. These switches are large, costly and exhibit poor rf performance at higher frequencies. The electro-mechanical switch has one feature that greatly adds to antenna selection reliability however; if the computer control section of the switch fails, the operator can rotate the switch to the desired position from the antenna switching front panel for rf path selection. Because of the many switch wafers and contacts

involved for proper switch operation, failures can be experienced from contact fatigue and contamination. Solid-state switching offers reduced losses at rf frequencies over rotary solenoid-activated switches due to fewer and less severe discontinuities.

There are two primary solid state methods for switching rf. In the receive mode, P-N diodes are adequate for rf switching. Since the receive signal levels are low (+10 dBm third-order intercept), low-power biasing is adequate. Diode bias must be set such that the rf signal level does not reverse bias the diode, introducing distortion. The dc bias power must not be less than the rf input power.

The second solid-state switching technique is PIN diodes. When switching rf power between 100 and 1000 watts average power, it becomes difficult to supply the diode switching networks with 100 to 1000 W of dc bias as in P-N diode use. PIN diodes exhibit characteristics whereby low dc biasing (on the same order of magnitude as the receive bias) can be implemented with low distortion.

2. Insertion Loss and Isolation Calculations

A seven-position single-pole switch has been built to the specifications shown in Table 1. The schematic is shown in Fig. 1, and the PIN diode model for a single position switch is shown in Fig. 2. In the "on" mode, (switch closure), the value of R is approximately 0.852 Ω. Within the 2–30 MHz frequency range, Cl can be neglected. The "on" insertion loss from the switch is calculated as follows: The voltage at the load without the switch is equal to

$$V_L = \frac{\text{load impedance}}{\text{load impedance plus source impedance}}. \quad [1]$$

Table 1—Specifications for 7-Position HF Switch.

Specification	Value
Power Handling Capability	1000 W Max.
Max. No. of Positions	7
DC Current (On Mode)	300 ma Max.
Max. RF Voltage (Z_0 = 50 Ω)	450 V_{RMS} Max.
Max. RF Current (Z_0 = 50 Ω)	8.90 A Rms. Max.
Off Insertion loss	25 dB Min.
On Insertion loss	.5 dB Max.
Manual Backup Capability	Yes
Diode Failure Indicator	Yes
Manual Override Indicator	Yes
Redundant Channel Lockout	Yes
Reverse Bias	−400 V Max.
Intermodulation Distortion Products (Two Tones 0.2V ea.)	> 60 dB
Package	Stud Mount Cathode to Stud

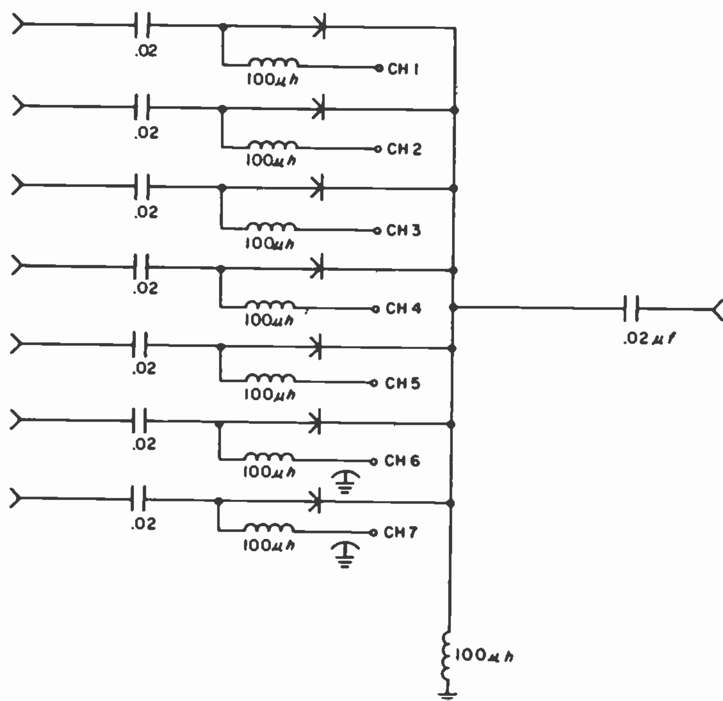

Fig. 1—HF switch configuration.

The voltage at the load after insertion of a PIN diode is

$$V_S = \frac{\text{load impedance}}{\text{load impedance plus source impedance and diode resistance}}. \quad [2]$$

The difference in dB is

$$\Delta_{\text{dB}} = \frac{20 \log V \text{ load without diode}}{V \text{ load with diode}}. \quad [3]$$

In a 50-Ω system the equation reduces to:

$$\Delta_{\text{dB}} = \frac{20 \log 100}{100 + \text{diode resistance}}.$$

The insertion loss using 0.8-Ω diode resistance is 0.07 dB.

In the "off" mode, switch open, R approaches 10 KΩ. The impedance of Cl at 2 MHz becomes 26.5 KΩ. The insertion loss using Eqs. [1], [2], and [3] and neglecting Cl becomes

$$\frac{20 \log 100}{100 + 10\ \text{K}\Omega} \approx -40\ \text{dB}.$$

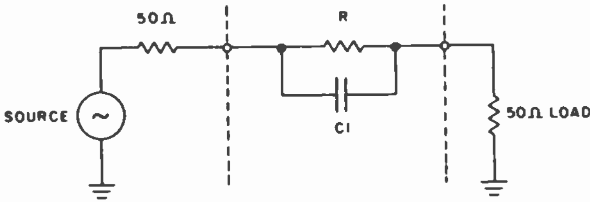

Fig. 2—PIN diode electrical model.

At 30 MHz, the impedance of CI becomes 1768 Ω. Again, using Eqs. [1], [2], and [3] and neglecting R1 and using the impedance of CI,

$$\frac{20 \log 100}{100 + 1768} \approx -26 \text{ dB}.$$

It is evident from these calculations that the "on" insertion loss will remain constant with frequency and is a function of the diode "on" resistance while the "off" insertion loss of the switch will vary with frequency and will be a function of the "off" capacitance of the diodes. If we relate these calculations back to the additional six sections constructed, these calculations are valid from any input port to the common output port. In the "off" position, the input-port-to-input-port isolation will increase by 6 dB. Having two input ports in the "on" position simultaneously is not a valid operational mode. Fig. 3 shows a plot of "off" isolation versus frequency.

The diodes for the 7-position switch (supplied by RCA Labs and discussed in Sec. 4) are housed in a stud-mounted package for ample heat transfer. Fig. 4 shows the diodes mounted in a circular heat sink. The heat sink is capable of dissipating the heat generated by the rf resistive losses of the diode through the front panel and by still-air convection. If 0.852-Ω diode resistance and 4.5 amperes RMS current for 1000-watt HF operation is assumed, there will be 16.2 watts of heat dissipation in the diode. All reactive losses due to load mismatch and switch reactances will not be converted to real power (heat), but to power reflected back into the source.

The manual override feature consists of a beryllium-copper contact that, when activated through a push-to-turn motion, will short the diode anode to the heat sink completing the rf path for that switch position. There is no provision for opening a diode faulted in the shorted mode. If a diode should fail in the shorted mode, which is highly unlikely with high rf power levels, another switch position can be selected with some degraded VSWR performance. The manual override capability can also be used for switch position selection if the PIN-diode computer control circuitry fails.

Diode switching can achieve performance surpassing a mechanical

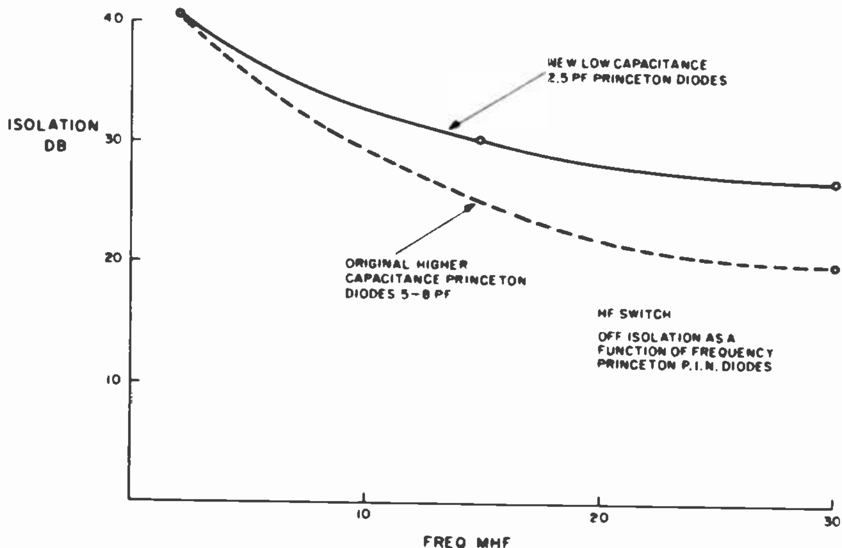

Fig. 3—"Off" isolation versus frequency.

rotary switch by exhibiting low "on" loss, acceptable VSWR, and high "off" isolation. Diodes require no moving contacts for switch closure, but with proper design, the mechanical override capability of the solenoid actuated switches can be duplicated to a large extent.

Two solid-state feasibility switch assemblies have been built and tested, one for HF and one for UHF.

3. High-Frequency Configuration

To prevent rf rectification at high power and lower rf frequencies (i.e., 2 MHz), longer minority-carrier-life-time PIN diodes are needed. RCA Laboratories at Princeton, NJ has developed PIN diodes which have carrier lifetimes of, typically, 30–50 μs (see Sec. 4). Commercially available units have a lifetime in the order of 4–10 μs maximum and their lowest usable frequency at high power levels is above 20 MHz. The first quantity of diodes developed for this application showed 8 pF capacitance in the "off" mode. The switch could achieve 20-db isolation; the requirement being 25 dB. A later quantity of improved diodes had only 2.5 pF capacitance and produced 26.5 dB isolation. The design trade-off was an increase in "on" resistance from a 0.4 to 0.852 ohm, which did not adversely affect switch operation (insertion loss is acceptably low).

The control circuitry for mode switching has 5 functions:

(1) Turn on selected switch position;

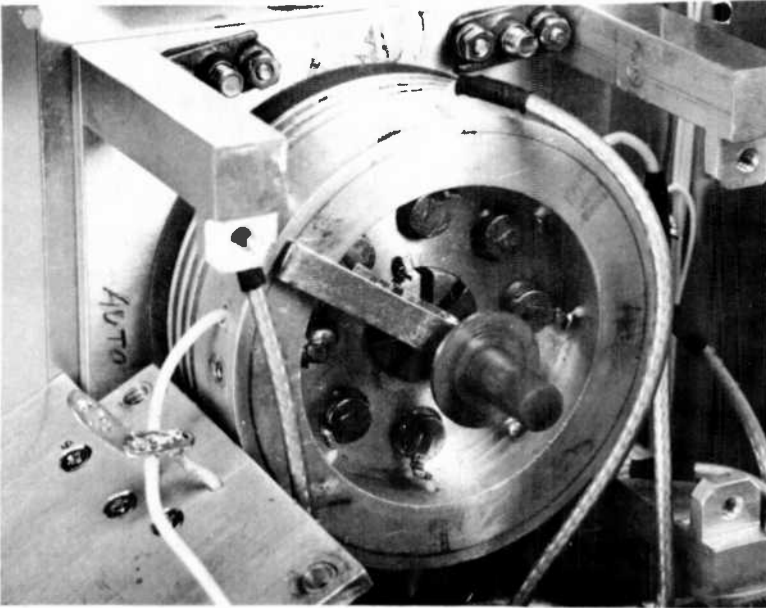

Fig. 4—Developmental HF switch with diodes in heat sink.

(2) Turn off switch positions not used;
(3) Monitor faulted diodes;
(4) Monitor manual override feature;
(5) Translate data to and from the switch through ASCII serial interface.

(1) Turn On Function

Fig. 5 is a block diagram of the interface circuitry. When a switch position is selected, 100 ma forward dc current is supplied to the diode, reducing the forward PIN diode resistance to the value of 0.8 Ω used in previous loss calculations.

(2) Turn-off Function

All nonselected diodes will be reversed bias at −400 V. Long-carrier-

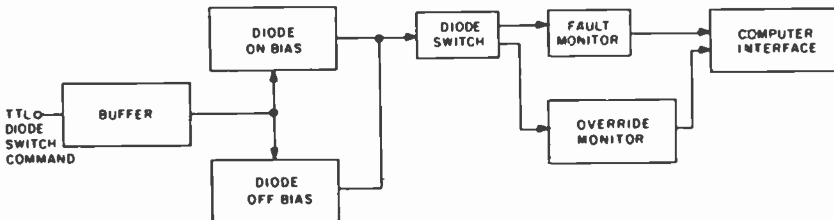

Fig. 5—Typical PIN diode switch block diagram.

lifetime PIN diodes display a characteristic whereby forward rf conduction will take place if the peak rf voltage exceeds the reverse bias voltage. This characteristic is present at lower rf frequencies (2 MHz) and changes gradually to conventional PIN diode behavior (low reverse-bias voltages) as the frequency increases. Above 60 MHz, 10 volts is adequate for PIN diodes turnoff. The peak rf voltage at 1000 watts rf power into 50 Ω is 320 V. Including mismatched conditions, −400 V is adequate to sustain the switch in the off condition at the lower rf frequencies.

(3) *Fault Diode Monitor*

Detection of faulted diodes (rf open or short) is essential when manual back-up systems are employed. The control circuitry monitors a selected diode for 1-volt forward bias. If the diode shorts, the voltage across the diode will go to 0; if the diode opens, the voltage will go to +5 V. When a fault is sensed, all diode selection commands from that individual switch are disabled, and the operator is notified of the faulted diode.

(4) *Manual Override Feature*

Selecting a diode manually mechanically shorts anode to cathode of the diode selected, completing the rf path. When the manual selection switch is in the auto mode, computer diode-selection commands are enabled. When the manual selection switch is moved away from the auto switch position, the computer diode-selection commands will be disabled and the computer operator will be notified of manual command and also which switch position is in manual override. Fig. 6 shows switch selection indicators, fault indicators, and manual selection switch.

(5) *ASCII Serial Interface*

A two-wire line using RS232 logic levels commands the switch. The ASCII serial interface format is shown in Fig. 7 for commanding switch position selection, and Fig. 8 shows the format for computer monitoring of switch status. Since the ASCII format has 8 serial characters, one character can be assigned to command each of 7 channels. To monitor bits, the information is coded using 10-line to 3-line TTL coding logic, which the computer is programmed to recognize. The switch command data is sent only once when a channel change is needed. Latches in the ASCII receiver will hold this data until another command is received. Switch monitor status is relayed back to the computer at a 300-ms rate.

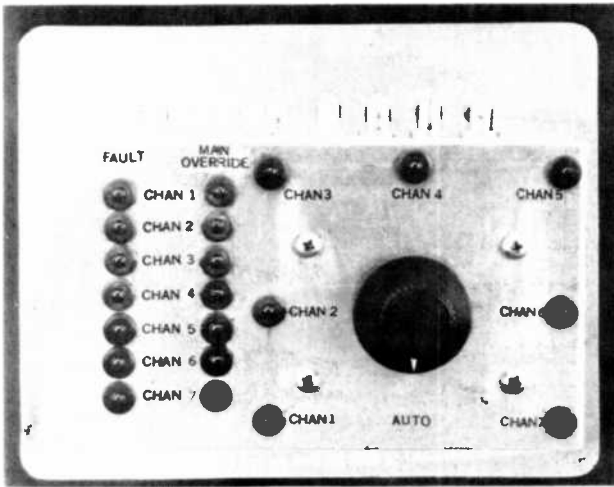

Fig. 6—PIN diode switch front panel.

4. PIN Diode Design Considerations

PIN diodes have been used as switches at microwave frequencies for many years.[1] Their use at HF frequencies is a novel application. We have been studying: (1) the requirements for reverse and forward-bias operation at low frequency and (2) design and fabrication of diodes to meet these requirements. The results of this study have been reported at the 1981 International MTT Symposium[2] and are the subject of a forthcoming detailed paper.[3]

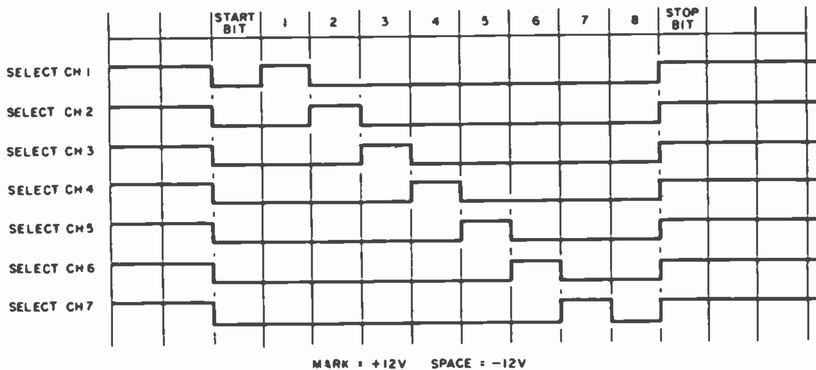

Fig. 7—PIN diode switch serial channel select format.

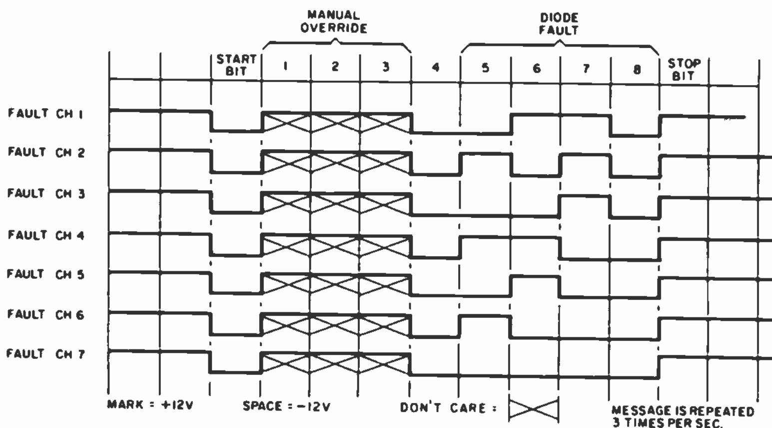

Fig. 8—PIN diode switch manual override and fault monitor serial data format.

We can summarize some important points here. In order to operate at high rf power at low frequency in the forward-bias mode, the carrier lifetime of the PIN diode must be made as large as is practical for fabrication. The results of our study reviewing past experience lead us to current guidelines for diode design.

A serious limitation for low-frequency operation is a requirement for large reverse-bias voltages. At microwave frequencies, the bias voltages need only be large enough to deplete the junction; at low frequency, the bias must be large enough to keep the rf voltage swing from extending into the forward conduction region. This limits the reverse-breakdown switch voltages.

We will first discuss PIN diode fabrication and design considerations to obtain long lifetime, which is necessary for low-distortion switches. Next, we will consider the reverse-bias limitation imposed by low-frequency applications.

4.1 Fabrication and Design

The low-frequency performance in forward-bias conditions is dependent on the lifetime achieved in the diode, as pointed out earlier. Lifetime and storage-time measurement procedures and dependent parameters have been discussed by Rosen et al.[1,4] The lifetime of a PIN diode is limited by carrier recombination, which depends on recombination (1) in the bulk, (2) at the surface of the n-layer sidewalls, and (3) at the n-n^+ and n-p^+ interfaces.

Surface recombination dominates. Fig. 9 is a plot of lifetime versus diode diameter, showing that increasing the diameter gives a significant increase in τ_e. Unfortunately increasing the diode diameter increases

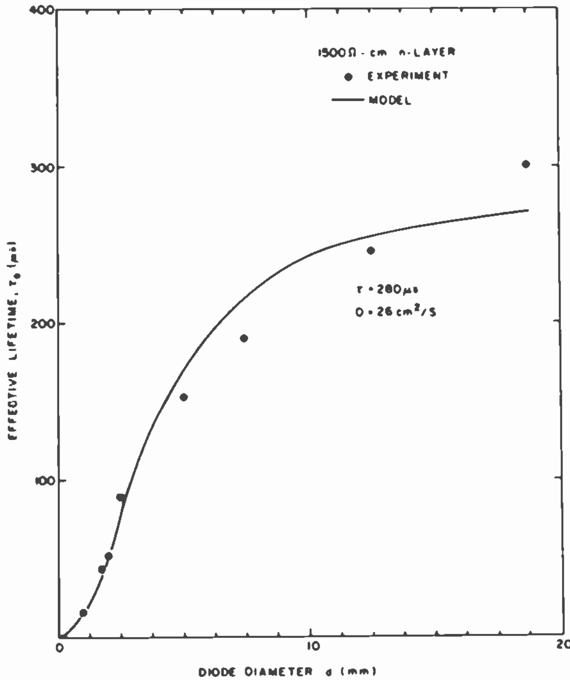

Fig. 9—Lifetime versus diode diameter.

the capacitance, which brings about a lowering of isolation in switches. The improvement in lifetime with diameter and accompanying increase in capacitance is one of the compromises required in diode design.

One technique used to permit increasing diode diameter (and thus the lifetime) while keeping the capacitance within limits is to stack diodes in series.[1] The stacked diode comprises two diodes in series. This reduces the capacitance as the number of diodes, n, but increases the thickness by nW and the resistance by nW^2 rather than $(nW)^2$. Another advantage of combining diodes is the possibility of increasing reverse-voltage breakdown. It is important to combine identical diodes, and the batch-fabrication technique described in Ref. (1) ensures better yield in this respect.

PIN diode interfacial recombination is higher than that in the bulk silicon. On that basis, it was proposed to increase the I-layer thickness so that the interface boundaries are more widely separated. A series of wafers of varying thicknesses were prepared and diodes of different diameters were fabricated.

Table 2 lists the lifetimes measured as a function of I-layer thickness and nominal diameters. With the mask used it was difficult to obtain many samples of 200-mil diodes and the values are averages. Over nine

Table 2—Lifetime τ_e Versus I-Layer Thickness for Three Diode Diameters

I-Layer Thickness	τ_e (μs)		
	D = 50 mils	D = 100 mils	D = 200 mils
4.4	13.0	20.1	31.1
5.	14.1	23.4	36.2
6.2	20.6	35.8	53.5
7.	21.2	42.	60.
8.5	23.0	33	
11	26	47	72

diodes of the smaller diameter were available for measurement on each wafer. As may be observed, the lifetime increased by a factor of two with thickness increases of 200%. Also, the capacitance decreased and voltage breakdown increased. The series resistance of a 12–13 mil thick diode, 65-mils in diameter, was measured to be on the order of 0.3 Ω.

A serious problem was encountered in attempting to fabricate mesa diodes from these thick substrates. Scribing and sawing the diodes apart was found to (1) degrade the lifetime and (2) cause leakage and lower voltage breakdown. Laser scribing was used in overcoming this problem.

A summary of design changes and their effects on diode performance is given in Table 3.

4.2 Reverse-Bias Operation

Fig. 10 schematically depicts the I–V characteristics of a PIN diode, showing reverse breakdown, zero bias, and applied reverse bias. Operation at a high rf voltage is shown with the voltage swing going in the

Table 3—PIN Diode Design Changes and Their Effect on Lifetime, Forward-Series Resistance, Reverse-Voltage Breakdown, and Capacitance

Design Change	Consequences
Increase I-Layer Thickness	Increases: Lifetime, Forward-Bias Resistance, Reverse-Voltage Breakdown, Processing Difficulties Requires Laser Scribing
Increase Diode Diameter	Increases: Lifetime, Capacitance
Combine Two Diodes Maintaining Wafer Thicknesses	Increases Breakdown Voltage Increases Forward Resistance Decreases Capacitance
Combine Two Diodes Reducing Wafer Thicknesses to ½	Reduces Series Resistance Decreases Lifetime Voltage Breakdown and Capacitance Unchanged

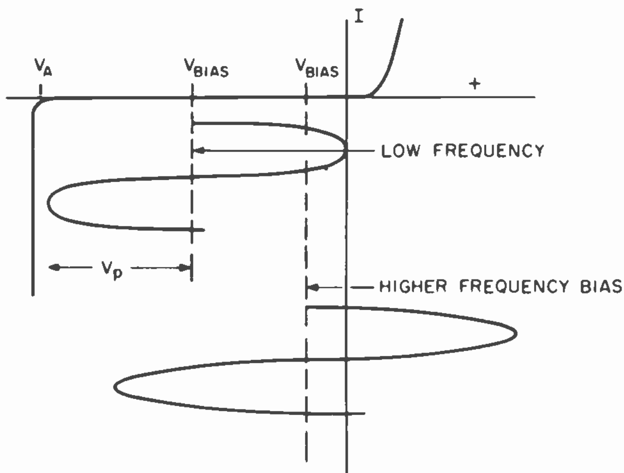

Fig. 10—Reverse-bias waveforms. Low and high frequency voltage swings superimposed on the I–V characteristics of the PIN diode.

forward conduction region (see lower swing labeled high frequency). According to White,[5] the rf voltage swing in the forward region is allowable within limits; no carriers reach the electrodes because the period of the swing is too short. However, impact ionization can occur and the voltage swing should be limited.

At low frequency, the application of a reverse bias voltage equal to the largest expected peak rf voltage (1.4 V_{rms}) is required. As can be seen in Fig. 10 for low-frequency operation, the rf voltage is limited to one-half of that of high-frequency operation. Experimentally, it was shown that the diode would burn out with less bias or more rf voltage.

A simple step-up transformer was constructed to test the diodes at different frequencies (under reverse-bias conditions). By setting up a voltage transformer across the diode, we were able to measure the voltage as the frequency was increased. As expected, at higher frequencies (>40 MHz) the rf voltage could penetrate the forward conduction region.

In summary, the criterion for operation at low frequencies is that the bias voltage must be at least equal to the peak voltages to keep the rf voltage swing from going into the positive region. Unfortunately, this lowers the p-p rf voltages to values below the reverse breakdown voltage. At higher frequencies, maximum allowable p-p rf voltage would be close to twice the reverse breakdown voltage.

The requirements for the operation of PIN diodes at low frequency and high power have been studied. A long lifetime diode is an important requirement for distortion-free operation.[6] Operating conditions (rf and bias current) must also be appropriate. Techniques to improve the lifetime, such as increasing diode diameter and I-layer thickness, allow

successful compromises with increasing capacitance and series forward resistance. An important consideration at low frequency is the reverse bias voltage needed to keep the reverse voltage swing from penetrating the forward conduction region. This in turn limits the voltage swing allowed and requires higher-voltage bias supplies.

5. UHF Switch

PIN diodes at UHF frequencies (225–400 MHz) are not critical in their design. There are presently several manufacturers who can meet the requirements for these switches. Table 4 gives the specifications for a 7-position UHF switch, and the schematic is shown in Fig. 11. The PIN diode model for a single position differs from that of the HF model in several ways. The "off" capacitance of the UHF diodes is on the order of 0.8 pF. At 400 MHz, this calculates to 497 Ω. Using the same configuration as the HF switch only, 14.75 dB isolation would be attainable. A second shunt diode must be added to each switch position.

The "on" resistance of a UHF PIN diode from 225 to 400 MHz is 1 Ω. With the series diode "off" and the short diode "on," the isolation of the switch at the load would increase to 48.9 dB. The 25 dB required will be exceeded by 23.9 dB. The added insertion loss due to the short diode capacitance will 0.4 dB with the switch in the "on" position.

To keep losses at a minimum, 50-Ω microstrip construction is used for all input and output ports. Fig. 12 shows the UHF switch with diodes mounted on a microstrip transmission line and a manual override feature. The override feature consists of a beryllium-copper contact, formed to the same width as the microstrip line. This minimizes transmitting-line discontinuities when in override. The mechanical activation of the manual override is a push-to-turn motion. Similar to the HF switch that connects diode anode to cathode.

Table 4—Specifications for 7-Position UHF Switch

Power Handling Capability	100–400 W
Max. No. of Positions	7
DC Current (On Mode)	300 mA Max.
Reverse Bias	−20 V Max.
Max. RF Voltage (Z_0 = 50 Ω)	300 V Max. RMS.
Max. RF Current (Z_0 = 50 Ω)	5.6 A Max. RMS.
Off Insertion Loss	25 dB Min.
On Insertion Loss	0.5 dB Max.
Manual Backup Capability	Yes
Diode Failure Indicator	Yes
Manual Override Indicator	Yes
Redundant Channel Lockout	Yes
Reverse Bias	−20 V Max.
Intermodulation Distortion Products (Two Tones 0.2 V each)	50 dB
Package	Microstrip Ribbon Leads

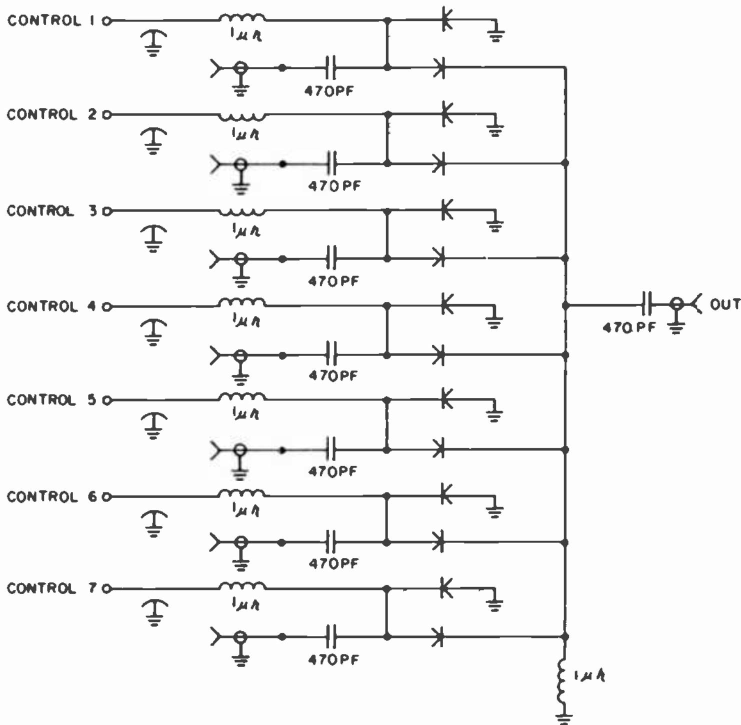

Fig. 11—Schematic of UHF switch.

The control circuit for the UHF switch is similar that for the HF, with the exception of the diode biasing. The UHF diodes do not require −400 V for diode turnoff, as required by the HF switch. Since a series shunt arrangement is used, +5 is required to turn on the series diode and turn off the shunt diode. Conversely −5 V is required to turn off the series diode and turn on the shunt diode to sustain switch "off" conditions. Diodes are supplied with 100-mA forward current.

Faulted diode monitor, manual override monitor, and ASCII serial interface is similar to that used for HF switch operation.

6. VLF Switch

VLF switch design requires "receive" only modes of operation. The switching configuration required is similar to HF and UHF (i.e., 7 positions).

PIN diodes are not required, nor applicable, at VLF frequencies. The minority-carrier lifetime required is not attainable at VLF. This application, requiring "receive-only" switching, readily lends itself to other modes of switching.

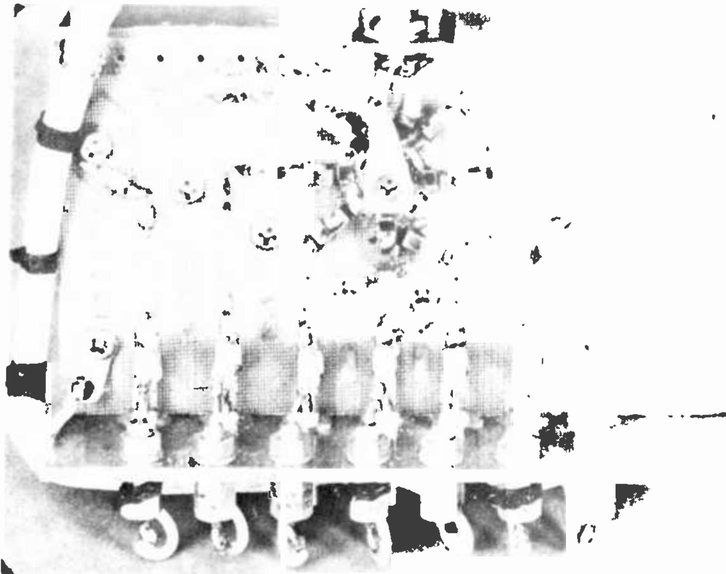

Fig. 12—UHF PIN diode microstrip layout.

A trade-off study was conducted to determine the best device approach. Transistors and diodes were both studied as possible devices. The transistor approach increases the rf levels that can be switched (better 3rd-order intercept) and provides easier methods of rf biasing. The noise figure of a transistor switch is an undesirable feature when switching VLF frequencies in the nanovolt range. The P-N diode approach requires more elaborate biasing to prevent losses, but does not degrade the noise figure by more than the insertion loss of the diode.

The diode approach was therefore chosen. A +20 dBm 3rd-order intercept was determined to be acceptable. This would allow undistorted signals up to a +10 dBm input. A P-N diode biased between the limits of rf excursion and with a 10-mA forward bias current will achieve this goal. If +10 dBm is required, the rf excursion will be +0.997 V volts peak-to-peak. The diode must be biased in a region where the rf voltage on the diode does not fall below the dc voltage on the diode. Improper bias would reverse bias the diode when in the "on" mode and create distortion through rectification.

Fig. 13 shows a schematic of a single position switch for evaluation. It should be noted that diode biasing is achieved with transistors. When biasing diodes at low frequenices, several problems must be overcome to obtain a low-loss switch. If the switch is biased inductively (a high shunt reactance for rf), the value and size of the inductors becomes large.

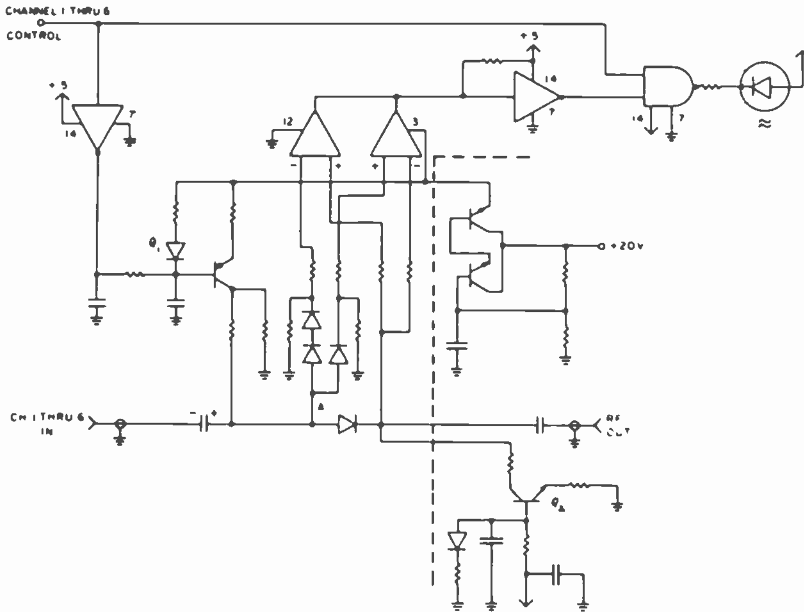

Fig. 13—VLF diode switch schematic.

Inductors also exhibit unwanted resonances. If resistor biasing is used, high resistor values are needed to obtain the necessary bias required for low loss. This mandates high bias voltages.

Transistor biasing achieves low loss and low bias voltage as follows. Both Q1 and Q2 can be expressed by the H parameter model shown in Fig. 14. Typical H parameters show that $h_{re}V_2$ can be neglected. Since $i = 0$, $h_{fe}i$ can be neglected. With operation at VLF and LF frequencies,

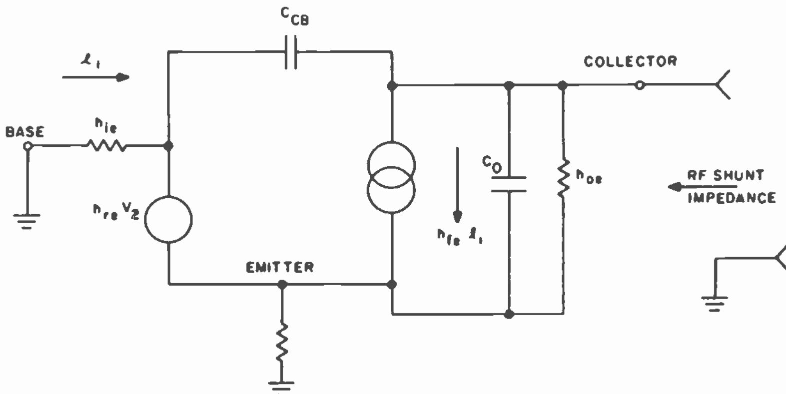

Fig. 14—Typical transistor H-parameter model.

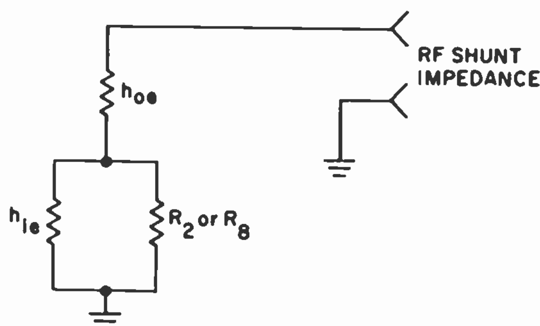

Fig. 15—H-parameter model reduction for diode switch bias.

C_{CB} and C_0 can be neglected. The model of Fig. 14 can now be reduced to that of Fig. 15. H_{oe} is high compared to the system impedance of 50 Ω. Therefore, system loss introduced by Q_1 and Q_2 will be on the order of 0.25 dB. The 7-position switch requires further evaluation, however, including noise figure measurements as well as diode distortion introduction.

7. Conclusions

Computer Selected Antenna switches using solid state devices at VLF, HF, and UHF frequencies must have each design addressed individually to obtain maximum rf switching efficiencies for that particular frequency range and power level. VLF or HF receive modes can be handled with P-N junction diodes. HF high power and UHF transmit/receive must be designed with appropriate PIN diodes. RF coupling and dc biasing techniques also differ among the different frequency ranges and are addressed individually.

The solid state switches have significant gains over the mechanical switches. They have no moving parts to deteriorate; they can be tailored to high efficiency transfer at UHF frequencies; and the *non*electronic switching of frequencies does not have to be sacrificed when converting to solid-state design. Manual override switching can be obtained with good rf integrity. The solid-state-switch dc control power is also lower, since the relatively high dc power (135 V at 1 A peak) needed to operate the solenoid on the mechanical switch is eliminated.

References:

[1] A. Rosen, R. U. Martinelli, A. Schwarzmann, G. J. Brucker, and G. B. Swartz, "High-Power, Low-Loss PIN Diodes for Phased-Array Radar," *RCA Review*, **40**, p. 22, March 1979.

[2] M. Caulton, A. Rosen, P. Stabile, and A. Gombar, "The Development of High-Power Low-Frequency PIN Diodes," *MTT-S International Microwave Symp. Digest*, Los Angeles, p. 255, June 15–19, 1981.

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[4] R. Martinelli and A. Rosen, "The Effects of Storage Time Variation on the Forward Resistance of Silicon p^+-n-n^+ Diodes at Microwave Frequencies," *IEEE Trans. Electron Devices*, **ED-27**, p. 1728, Sept. 1980.

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[6] A. Rosen, R. U. Martinelli, and M. Caulton, "Temperature Dependence of Storage Time in Silicon p^+-n-n^+ Switching Diodes and Reduction of Harmonic Distortion," *Electronic Letters*, **16**, p. 66–68, 17 Jan. 1980.

Automatic S-Parameter Characterization of Microwave Devices and Circuits Using a Phase Locked Automatic Network Analyzer (PLANA)

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RCA Laboratories, Princeton, NJ 08540

Abstract—PLANA/1000 is a software package designed for use with an HP-1000 disc-based minicomputer system to provide accuracy enhancement for the HP-8409 series of network analyzer systems. This paper describes the functional program characteristics and its operating capabilities, and gives examples of program uses. The program, written in Fortran IV, provides for hardware calibration, device measurement, complex vector mathematics and plotting of data output, disc and tape file management, an interactive operator interface, and control of the phase-locked frequency source subsystem and other instrumentation using the HP-IB (IEEE 488) interface.

1. Introduction

PLANA/1000 is a software package designed for use with a disc-based HP-1000 minicomputer system to provide accuracy enhancement for the HP 8409 series of network analyzer systems. In its standard configuration, PLANA/1000 embodies all of the concepts provided by the HP 11863D software package provided with calculator-based systems.

General Description

The PLANA/1000 software, written in FORTRAN IV, is specifically designed to control an HP 8409-Series Network Analyzer System* such as the one shown in Fig. 1. A block diagram of this system is given in Fig.

* Hewlett-Packard Co., 1400 Fountain Grove Pkwg., Santa Rosa, CA 95404.

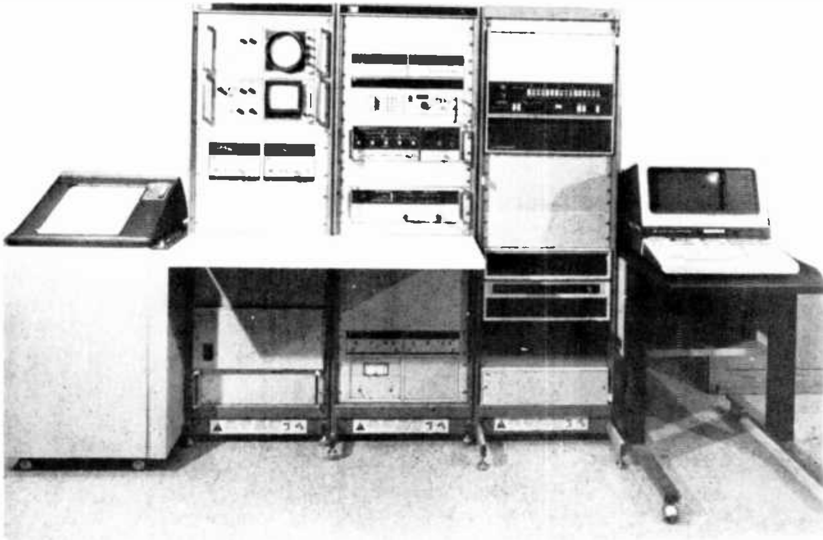


Fig. 1—A phase-locked automatic network analyzer system.

2. The program provides for hardware calibration, device measurement, complex vector mathematics, error correction of transmission and reflection measurements, listing and plotting of data output, disc and tape file management, an interactive operator interface and control of the phase-locked frequency source subsystem and other instrumentation using the HP-IB (IEEE 488) interface.

The program incorporates a choice between four (4) calibration error models in support of either the HP 8743A, HP 8745A or HP 8746B reflectometer. The 3-vector model provides for full error correction of reflection measurements on one-port devices, providing for directivity, source match, and frequency response vector error correction. The 6-vector model includes the 3-vector model plus frequency response for forward transmission, load match and isolation, for vector error correction of two-port devices but requiring device reversal to correct for all four S-parameters. The 12-vector model is essentially a 6-vector model for forward correction (i.e., S_{11}, S_{21}) and a 6-vector model for reverse correction (i.e., S_{22}, S_{12}), thereby permitting full error correction of a two-port device when an HP 8745 or HP 8746 reflectometer is used. A 1-vector transmission frequency response model is available for making simplified transmission measurements (i.e., S_{21}, S_{12}) for reasonably matched two-port devices where normalization of magnitude and phase frequency response errors provides sufficient accuracy. This latter model may be combined with the 3-vector reflection model to produce a 4-vector model for accurate reflection measurements with fast transmission measurements.

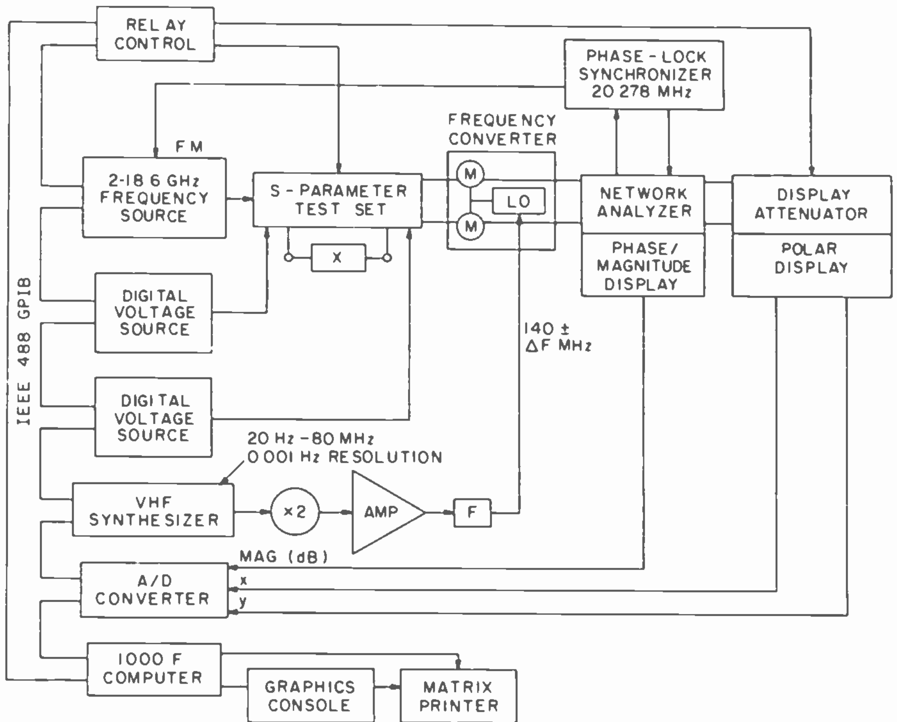


Fig. 2—PLANA system hardware.

The choice of model is interactive, allowing one to switch between models to achieve the highest possible accuracy or minimize switching errors and reduce measurement time. Additional procedures are available for characterizing two-port devices, particularly those with mixed connector types by using a sliding load and other standard terminations. Measurement resolutions of 0.02 dB in amplitude, 0.1° in phase, 0.1 ns in delay, and 100 Hz in frequency are achieveable. The group delay is obtained by calculating the derivative of the corrected transmission phase data with respect to frequency.

For measurement of devices using APC-7, Type N, APC-3.5, and SMA connectors, the standard reflection calibration sequence uses a short circuit and either a shielded open circuit or an offset short circuit to establish source match and frequency response error terms. The program allows the specification of the short position and the value of the open circuit capacitance or the length of the offset short. Standard lengths are used when requested, particularly when the frequency range covers more than one octave. Frequency dependent values for the open circuit capacitance are provided for each of the standard connector types. Best

results for calibration using two offset shorts is obtained when the frequency range is limited to less than an octave; the offset lengths should be $\frac{1}{8}\lambda$ and $\frac{3}{8}\lambda$, where λ is the test signal wavelength in the center of the octave range for the media in use.

Additional features of the program include adaptive averaging of measured data, automatic saving of calibration measurement data in a disc file, de-embedding of cascaded networks, frequency setting routines for either the HP 8620C or the HP 8350A Sweep Oscillator mainframe, and functional test and A/D converter calibration routines. The adaptive averaging technique improves system accuracy and repeatability by increasing the number of averaged measurements at each data point for low-level responses. Saving of the calibration and measurement data provides for convenient restoration of the data following any irreversable calculation or system failure. The de-embedding technique provides an accurate method for characterizing a network cascaded with premeasured input and/or output circuits. The functional test and A/D converter calibration routines provide a convenient method for checking each system instrument without having to load a separate program.

User options may be entered in alphanumeric format in order to direct program flow, from calibration to measurement, to list or plot, to change a particular procedure, to change frequency lists or reference planes, to save or restore the program's state, to smooth measured data, or to perform many other tasks. Outputs include S-parameters, VSWR, impedance and admittance, group and phase delay, as well as maximum available gain and stability of active two-port device. Output data may be smoothed and/or displayed graphically in either polar, S-chart, or rectangular format, listed to a terminal or line printer, or saved in a disc or tape file for use by other programs.

Controller Description

The use of an HP 1000 as the system controller represents the unique difference between the commercially available HP 8409B and what is described here. In one of its standard configurations (consisting of a computer, disc, and graphics terminal), the HP 1000 provides a powerful alternative to the HP 9845T which is normally provided as the 8409B controller. The disc-based minicomputer, supported by a user configured operating system such as RTE-4B with its optional session accounting software, permits program development in a high level language such as FORTRAN IV and the use of multiple PLANA type systems, as well as multiple terminals and printers. The multiprogramming features of RTE-4B permits on-line editing and compiling, with concurrent execution of other programs while the PLANA program is actively taking

measurements. Perhaps the single most significant advantage in using the HP-1000 as the PLANA controller is the ease of establishing a data base of corrected measurement data and accessing that data from other programs and terminals such as those used for CAD (computer aided design).

The controller and system configuration, shown in Fig. 3, was used in the design and implementation of the PLANA software. In this case, an HP 1000F was used where the 'F' signifies the use of the HP 2117 mainframe, which incorporates a hardware floating point processor, in addition to SIS (scientific instruction set) and VIS (vector instruction set) firmware. These special capabilities are of particular significance in improving computational speed in support of CAD software used on the same system. The CPU was supported by 512 Kbytes of semiconductor memory, 20 Mbytes of disc memory, and a real-time clock.

The HP 2648A video graphics terminal provides an interactive input/output device for displaying alphanumeric text, program prompting, and/or raster graphics with a pixel resolution of 360 × 720. Corrected measurement data may be displayed in polar, S-chart, or rectangular format. These terminals also support magnetic tape cartridges with a capacity of 220 Kbytes for off-line storage. In this development configuration, hardcopy printout was obtained by listing output data for Versatec* matrix printer with a throughput of 1000/lpm or to a HP 2635B 180 cps printer/terminal. The Versatec printer also provides a means to obtain hardcopy graphics by directly copying the image displayed on either of the graphics terminals in approximately 8 sec or producing high resolution (160 dots/inch) graphics under software control. An HP 7310A Printer could be used as an alternative graphics image copying and list device.

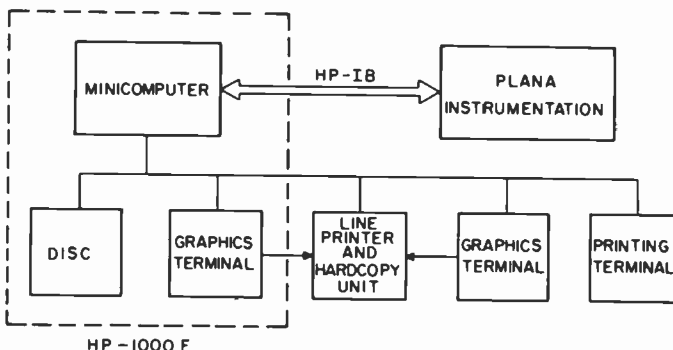


Fig. 3—System configuration for using the PLANA instrumentation with an HP-1000 computer.

* Versatec, a Xerox Company, 2805 Bowers Ave., Santa Clara, CA 95051

Program Design

The program PLANA is written in FORTRAN IV and designed to run on a disc-based HP 1000 under the control of the RTE-4B operating system. It consists of a main program and six overlapping program segments, as shown in Fig. 4, that communicate between each other through a common memory area. A memory partition of at least 20 pages (40 Kbytes) is required to support the loaded program. This design provides the means for supporting up to 81 test frequencies and 12 error correction vectors, without the need for hard storage (i.e., tape or disc) during the calibration or measurement routines, while also providing the user with a variety of interactive options. The segmentation philosophy also lends itself to a convenient means to expand the program's capabilites by simply expanding existing segments or adding new ones.

The program is designed to perform four primary tasks: (1) calibrate, (2) measure, (3) list, and (4) plot. Segments 1–4 are substantially relegated to these tasks with segment 5 providing file management of common state variables. The main program, almost entirely a common block, links with each of the segments. Segment Ø is used primarily to interpret the user's requests and schedule the appropriate segment to carry out the task. Segment 6 is reserved for future enhancements. A detailed description of the function of each sement is given below:

PLANØ—This segment contains the mnemonic task interpreter which is used to direct program flow, select an output and a list device. Other functions include initializing the calibration procedure,

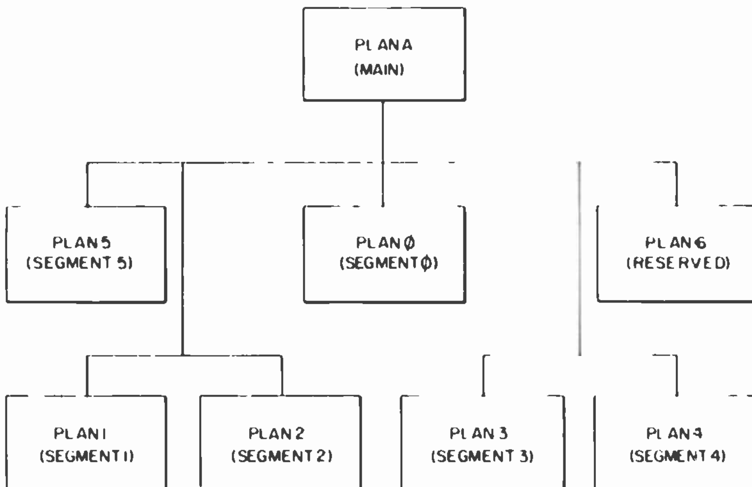


Fig. 4—Program segmentation scheme used by PLANA.

reading measurement frequencies, changing output list frequencies, reference planes, error model or instrument settling delay. Program control returns here following each task.

PLAN1—This segment contains the error vector calibration procedure as well as calibration of the polar display, instrument diagnostics and control, including setting a single or digitally swept frequency, switching reflectometer S-parameters, relay actuator control and returning the HP-IB (IEEE 488) bus to local mode.

PLAN2—This segment is responsible for performing the actual measurement by acquiring data from the device under test and reducing that data using the appropriate error correction algorithm. Another function is continuous processing and display of corrected data for realtime measurements. S-parameter data smoothing is also performed here.

PLAN3—This segment formats data output to be listed on any terminal, line printer, magtape or disc file. The disc file can be located locally or on any active node within a network which supports DS-1000 and contains the PLANA controller. Any combination of two (2) columns of listed data can be plotted using the autoplot feature of the HP 2648.

PLAN4—This segment provides for soft and hardcopy graphics using either the HP 2648 video terminal or the HP 9872 4-color plotter. Polar, Smith chart, or rectangular formats are available for the HP 2648, while the HP 9872 is only supported for data output to preprinted Polar and Smith charts. Graphics data may be smoothed before output without affecting the S-parameter data.

PLAN5—This segment provides for saving or restoring program common using a state file on disc. Another function is the deembedding of an input and/or output network using appropriate pre-measurement data files.

PLAN6—Reserved for future program enhancements.

The program is modular in its design, utilizing subroutines to perform specific tasks such as controlling individual instruments, computing quadrature error coefficients for calibrating the polar display, acquiring polar display dc offsets for the beam center calibration, modeling the open circuit capacitance, parameter selection, rotating reference planes, creating disc files, scaling, smoothing, plotting, etc. Modifications to the software in order to suit changes in configuration or procedure are readily performed by replacing the appropriate subroutine. Unique and extensive data reduction or special programming requirements can be readily implemented by adding new segments.

Controller Requirements

PLANA/1000 was designed for use with an HP-1000 having at least 192 kbytes of memory (256 kbytes is preferred), a suitable disc and at least one HP-2648 graphics terminal. RTE-IVB is the preferred operating system, although the program may easily be modified to run on other RTE systems. An HP-59310B bus controller is also required. Other peripherals, such as a line printer, hard-copy unit (e.g., Versatec 1640), a flatbed plotter, or the use of DS/1000, are optional.

Examples of Printed and Plotted Output

The following printouts and plots demonstrate the variety of output formats available. Data taken on two different 2-port devices was chosen for clarity in presenting these examples. In both cases, an HP 8746B test set was used with the FULL (4) or twelve (12) error vector model chosen to provide full error correction. The local terminal used was an HP 2648A.

Use of VI Task Modification

The corrected frequency response data for the forward gain (i.e., $S21$ in dB) of a three section bandpass filter is given in Fig. 5. This particular device was measured at 81 discrete frequencies from 8600 MHz to 9400 MHz with a step size of 10 MHz. The video graphics result shown was invoked with TASK? = VI, S21-dB.

The passband response for the filter characteristic shown in Fig. 5 may be expanded to display more detail by changing the output frequency list to

START, STOP, STEP (MHz)? = 8900, 9100, 10

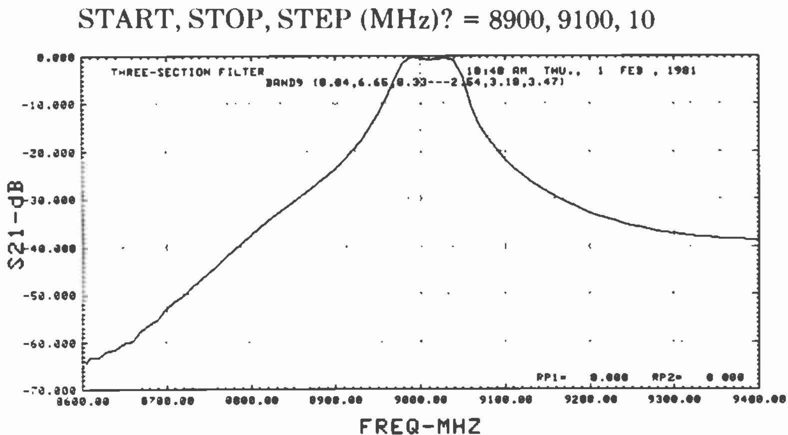


Fig. 5—Frequency response of bandpass filter.

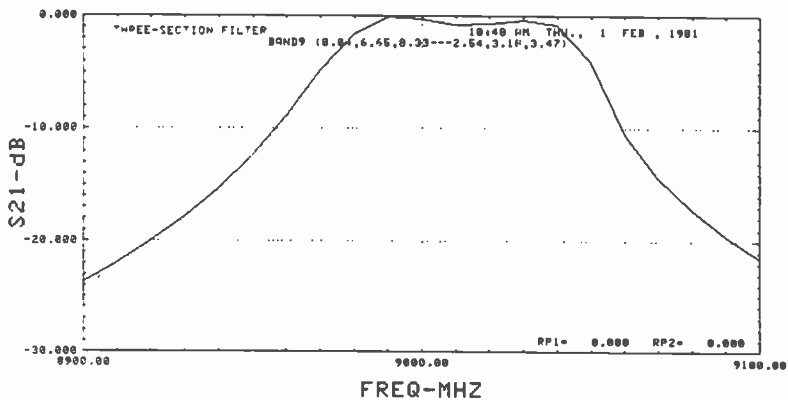


Fig. 6—Expanded frequency response of bandpass filter.

and reissuing TASK? = VI, S21-dB. The result is given in Fig. 6. The corresponding Smith chart display for S11 is given in Fig. 7 using TASK? = VI, SM; TASK? = VI, PD and TASK? = VI, S11. This result can be expanded using a Polar plot with the result given in Fig. 8 using TASK? = VI, PO and TASK? = VI, S11. In this case the polar radius has been changed automatically from 1.0 to 0.3.

Use of LI Task Modification

The modified output list of S-parameters for the three section filter obtained by using TASK? = LI, SP, is given in Listing 1. Listing 2 gives the magnitude data in dB using TASK? = LI, SD.

The input reflection and immittance data for an FET test cell, mea-

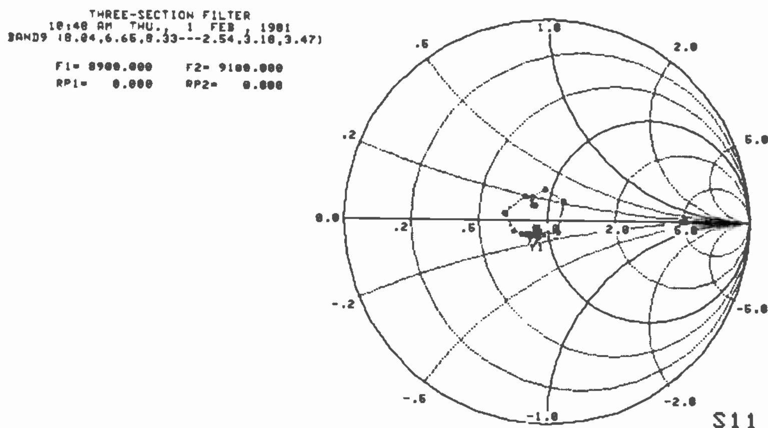


Fig. 7—Smith chart display of S11.

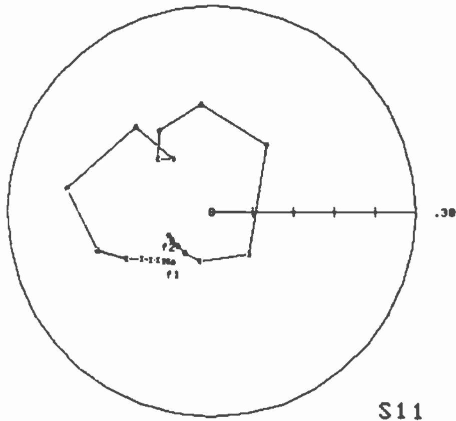


Fig. 8—Polar chart display of S11.

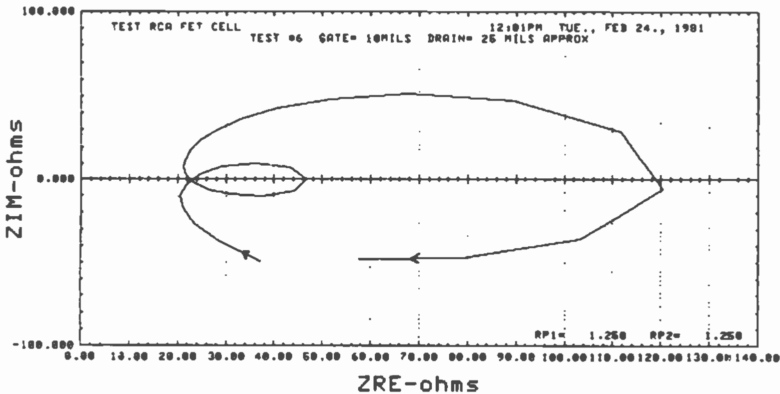


Fig. 9—Bode plot of Z_{in} for the FET test cell.

sured over the frequency band from 12,000 MHz to 16,000 MHz, is given in Listing 3. This particular list was obtained using TASK? = LI, SZ.

Using the PL Task Modification

The output data for the input characteristics of the FET test cell, Listing 3, may now be used to demonstrate the use of TASK? = PL. The Bode plot of $\text{Im}(Z_{in})$ versus $\text{Re}(Z_{in})$ given in Fig. 9 is obtained by specifying TASK? = PL, SZ. The appropriate prompts and responses are

NEW PLOT? (Y/N) Y
Xcol, Ycol, Ltype? = 6, 7, 1
Change AUTOPLOT MENU? (Y/N) Y

Changing the AUTOPLOT MENU was selected in order to change the

THREE-SECTION FILTER 10:48 AM THU., 1 FEB , 1981
BAND9 (8.04,6.65,8.33---2.54,3.18,3.47)

FREQ(MHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
8900.0000	.094	-127.4	.066	-66.4	.066	-66.4	.094	-127.4
8910.0000	.097	-130.9	.080	-77.0	.080	-77.0	.097	-130.9
8920.0000	.102	-134.6	.100	-87.3	.100	-87.3	.102	-134.6
8930.0000	.108	-138.1	.128	-98.1	.128	-98.1	.108	-138.1
8940.0000	.114	-141.9	.171	-108.9	.171	-108.9	.114	-141.9
8950.0000	.125	-146.0	.239	-121.0	.239	-121.0	.125	-146.0
8960.0000	.144	-151.0	.361	-136.3	.361	-136.3	.144	-151.0
8970.0000	.179	-161.4	.567	-161.4	.567	-161.4	.179	-161.4
8980.0000	.216	170.7	.831	158.8	.831	158.8	.216	170.7
8990.0000	.168	131.8	.993	108.5	.993	108.5	.168	131.8
9000.0000	.097	126.9	.968	64.5	.968	64.5	.097	126.9
9010.0000	.111	135.7	.914	36.8	.914	36.8	.111	135.7
9020.0000	.142	123.3	.933	14.1	.933	14.1	.142	123.3
9030.0000	.157	96.1	.960	-13.7	.960	-13.7	.157	96.1
9040.0000	.127	50.2	.922	-54.4	.922	-54.4	.127	50.2
9050.0000	.084	-48.0	.634	-125.3	.634	-125.3	.084	-48.0
9060.0000	.076	-103.7	.301	-162.3	.301	-162.3	.076	-103.7
9070.0000	.072	-123.2	.193	-174.0	.193	-174.0	.072	-123.2
9080.0000	.072	-135.5	.139	176.6	.139	176.6	.072	-135.5
9090.0000	.073	-144.6	.106	168.4	.106	168.4	.073	-144.6
9100.0000	.074	-152.1	.084	160.8	.084	160.8	.074	-152.1

Reference Planes: RP1= 0.000cm, RP2= 0.000cm

List 1—S-parameters (Mag, Angle) for bandpass filter.

THREE-SECTION FILTER 10:48 AM THU., 1 FEB , 1981
BAND9 (8.04,6.65,8.33---2.54,3.18,3.47)

FREQ(MHz)	S11		S21		S12		S22	
	DB	ANG	DB	ANG	DB	ANG	DB	ANG
8900.0000	-20.56	-127.4	-23.62	-66.4	-23.62	-66.4	-20.56	-127.4
8910.0000	-20.25	-130.9	-21.91	-77.0	-21.91	-77.0	-20.25	-130.9
8920.0000	-19.80	-134.6	-19.98	-87.3	-19.98	-87.3	-19.80	-134.6
8930.0000	-19.34	-138.1	-17.83	-98.1	-17.83	-98.1	-19.34	-138.1
8940.0000	-18.86	-141.9	-15.35	-108.9	-15.35	-108.9	-18.86	-141.9
8950.0000	-18.03	-146.0	-12.41	-121.0	-12.41	-121.0	-18.03	-146.0
8960.0000	-16.84	-151.0	-8.86	-136.3	-8.86	-136.3	-16.84	-151.0
8970.0000	-14.96	-161.4	-4.93	-161.4	-4.93	-161.4	-14.96	-161.4
8980.0000	-13.31	170.7	-1.61	158.8	-1.61	158.8	-13.31	170.7
8990.0000	-15.50	131.8	-.06	108.5	-.06	108.5	-15.50	131.8
9000.0000	-20.29	126.9	-.28	64.5	-.28	64.5	-20.29	126.9
9010.0000	-19.11	135.7	-.78	36.8	-.78	36.8	-19.11	135.7
9020.0000	-16.98	123.3	-.61	14.1	-.61	14.1	-16.98	123.3
9030.0000	-16.08	96.1	-.36	-13.7	-.36	-13.7	-16.08	96.1
9040.0000	-17.92	50.2	-.71	-54.4	-.71	-54.4	-17.92	50.2
9050.0000	-21.49	-48.0	-3.96	-125.3	-3.96	-125.3	-21.49	-48.0
9060.0000	-22.43	-103.7	-10.44	-162.3	-10.44	-162.3	-22.43	-103.7
9070.0000	-22.81	-123.2	-14.31	-174.0	-14.31	-174.0	-22.81	-123.2
9080.0000	-22.84	-135.5	-17.11	176.6	-17.11	176.6	-22.84	-135.5
9090.0000	-22.79	-144.6	-19.50	168.4	-19.50	168.4	-22.79	-144.6
9100.0000	-22.65	-152.1	-21.51	160.8	-21.51	160.8	-22.65	-152.1

Reference Planes: RP1= 0.000cm, RP2= 0.000cm

List 2—Magnitude data in dB using TASK? = LI, SD.

X-axis limits from $X_{min} = 20.0$ ohms to 0.0 ohms and $X_{max} = 13.0$ ohms to 140.0 ohms.

Applications

The automatic network analyzer configuration described here is well suited for many applications ranging from engineering research and development to computer aided manufacturing. Complementing the

network analyzer hardware with a powerful minicomputer controller such as the HP-1000 has provided great flexibility. In engineering design and development applications, such a system provides the user with a wide choice of options; while in a manufacturing environment, an on-line configuration option may be used to identify standard test procedures.

The range of microwave applications covers simple one-port measurements of VSWR on reflection coefficients to two-port measurements and characterization of active or passive devices in chip or packaged form, imbedded in a test fixture, or in a fully operational circuit assembly. More complex measurements involving the use of de-embedding techniques, characterization of multiport (>2 ports) devices (such as hybrids), and characterization of non-insertable devices (such as waveguide to coax geometries) are also supported. Calculation of group delay, maximum available gain, and stability is of interest to the circuit designer. Equally important is the ability to save empirical device results in a data base for use with CAD programs.

TEST RCA FET CELL — 12:01PM TUE., FEB 24., 1981
TEST #6 GATE= 10MILS DRAIN= 25 MILS APPROX

FREQ(MHz)	Reflection			VSWR	Z(ohms)		Y(mmhos)	
	MAG	ANG	DB		REAL	IMAG	REAL	IMAG
12000.0000	.508	-75.2	-5.88	3.064	37.14	-49.16	9.78	12.95
12125.0000	.495	-94.5	-6.11	2.958	28.55	-37.27	12.95	16.91
12250.0000	.482	-114.8	-6.34	2.859	23.47	-26.74	18.54	21.12
12375.0000	.462	-134.3	-6.71	2.718	21.16	-17.80	27.68	23.28
12500.0000	.435	-153.2	-7.22	2.542	20.60	-9.97	39.33	19.03
12625.0000	.394	-171.2	-8.09	2.301	21.83	-3.13	44.88	6.43
12750.0000	.345	171.1	-9.23	2.055	24.44	2.96	40.33	-4.88
12875.0000	.278	154.0	-11.12	1.770	29.26	7.73	31.94	-8.44
13000.0000	.195	137.9	-14.19	1.485	36.22	9.86	25.71	-7.00
13125.0000	.107	127.4	-19.41	1.240	43.30	7.45	22.43	-3.86
13250.0000	.033	176.0	-29.67	1.068	46.83	.21	21.36	-.10
13375.0000	.099	-124.4	-20.08	1.220	44.14	-7.29	22.06	3.64
13500.0000	.185	-133.2	-14.64	1.455	37.49	-10.50	24.73	6.92
13625.0000	.261	-147.0	-11.66	1.707	30.93	-9.45	29.57	9.03
13750.0000	.320	-160.4	-9.89	1.942	26.31	-6.30	35.95	8.61
13875.0000	.365	-174.0	-8.75	2.150	23.30	-2.05	42.59	3.74
14000.0000	.397	172.3	-8.02	2.319	21.64	2.75	45.47	-5.77
14125.0000	.416	158.9	-7.61	2.427	21.20	7.70	41.69	-15.13
14250.0000	.429	145.8	-7.36	2.501	21.56	12.73	34.40	-20.30
14375.0000	.438	132.6	-7.18	2.556	22.66	18.05	26.99	-21.50
14500.0000	.442	119.2	-7.08	2.587	24.72	23.75	21.04	-20.21
14625.0000	.441	106.0	-7.11	2.577	28.02	29.49	16.93	-17.82
14750.0000	.440	91.8	-7.13	2.572	32.99	35.99	13.84	-15.10
14875.0000	.437	77.1	-7.19	2.554	40.62	42.80	11.67	-12.29
15000.0000	.430	62.6	-7.34	2.506	51.67	48.33	10.32	-9.66
15125.0000	.424	47.4	-7.45	2.474	67.74	51.58	9.34	-7.11
15250.0000	.419	31.6	-7.55	2.443	89.27	47.56	8.73	-4.65
15375.0000	.415	14.9	-7.65	2.417	111.79	28.70	8.39	-2.15
15500.0000	.414	-2.9	-7.66	2.414	120.32	-6.01	8.29	.41
15625.0000	.409	-20.9	-7.76	2.387	103.37	-36.27	8.61	3.02
15750.0000	.405	-38.5	-7.86	2.359	78.78	-47.48	9.31	5.61
15875.0000	.411	-57.1	-7.71	2.398	57.47	-47.81	10.28	8.55
16000.0000	.411	-75.1	-7.73	2.393	43.44	-41.46	12.05	11.50

Reference Planes: RP1= 1.250cm, RP2= 1.250cm

List 3—Input reflection and immittance for FET test cell.

Patents Issued to RCA Inventors—Third Quarter 1981

July

B. Abeles Precoated Resistive Lens Structure for Electron Gun and Method of Fabrication (4,281,270)
M. S. Abrahams and J. Blanc Method of Improving Silicon Crystal Perfection in Silicon on Sapphire Devices (4,279,688)
H. W. Bilsky and P. J. Callen Redundant Battery Protection System (4,281,278)
T. J. Christopher PCM Detector for Video Reproducer Apparatus (4,278,992)
T. J. Christopher Stylus Position Sensing Apparatus for VideoDisc Player (4,280,023)
E. L. Crosby, Jr. Balloon With Deflation Port (4,280,674)
P. Datta and R. N. Friel Video Discs and Molding Compositions Therefor (4,280,941)
A. R. Dholakia Selectively Damped VideoDisc Stylus Assembly (4,280,024)
K. Fukazawa and A. Yamada VideoDisc Locked Groove Clearance System (4,278,846)
J. B. George Power Supply Arrangement for a Tuning System (4,281,349)
W. Hinn Automatic Kinescope Biasing System With Increased Interference Immunity (4,277,798)
S. T. Hsu Method for Forming Buried Contact Complementary MOS Devices (4,276,688)
S. T. Hsu Method for Forming an Improved Gate Member Utilizing Special Masking and Oxidation to Eliminate Projecting Points on Silicon Islands (4,277,884)
L. A. Kaplan Current Scaling Circuitry (4,278,946)
E. J. Nossen Range Determining System (4,278,977)
M. Packer Method for Releasing Printed Wiring Boards From Printed Wiring Board Racks (4,279,073)
R. N. Rhodes Color Filter Having Vertical Color Stripes With a Nonintegral Relationship to CCD Photosensors (4,277,801)
L. R. Rockett, Jr. Quantizing Circuits (4,280,191)
R. L. Rodgers, 3rd Simplified Vertical Deflection Circuit (4,277,729)
M. D. Ross Slow Down Color Processor for VideoDisc Mastering Using a Special Mode VTR (4,277,796)
H. I. Schanzer and R. G. Stewart Circuit for Reducing the Loading Effect of an Insulated-Gate Field-Effect Transistor (IGFET) on a Signal Source (4,281,400)
S. Tosima Surface Acoustic Wave Pickup and Recording Device (4,281,407)
S. T. Villanyi Cathode-Ray Tube Having Corrugated Shadow Mask With Varying Waveform (4,280,077)
P. P. Webb Photodiode Having Enhanced Long Wavelength Response (4,277,793)
L. K. White, R. B. Comizzoli, and G. L. Schnable Method of Detecting a Cathodic Corrosion Site on a Metallized Substrate (4,278,508)
J. A. Wilber and B. J. Yorkanis Amplifier Having Dead Zone of Controllable Width and Position (4,277,695)
B. F. Williams Method for Forming an Electrical Contact to a Solar Cell (4,278,704)

August

A. A. Ahmed Series Voltage Regulators for Developing Temperature-Compensated Voltages (4,282,477)
A. A. Ahmed Current Dividers Using Emitter-Coupled Transistor Pairs (4,284,945)
A. R. Balaban and S. A. Steckler Pulse Generator for a Horizontal Deflection System (4,282,549)
I. Balberg Silicon MOS Inductor (4,282,537)
H. R. Beelitz and D. R. Preslar Method of Integrating Semiconductor Components (4,282,538)
A. E. Bell Replicable Optical Recording Medium (4,285,056)
C. B. Carroll, F. C. Schaller, and A. E. Beres Automatic Apparatus for Molding a Preform (4,281,816)
T. J. Christopher and J. A. Wilber Periodically Biased VideoDisc Player Servo System (4,286,282)
J. K. Clemens Transcoder (4,286,283)
E. H. Delrio Means to Orbit and Rotate Target Wafers Supported on Planet Member (4,284,033)
J. R. Dinardo, Jr. Method for Fabricating Flyleads for VideoDisc Styli (4,282,311)
A. G. Dingwall Transition Detector Circuit (4,286,174)
A. W. Fisher Method for Determining Silicon Content in Layers of Aluminum and Silicon (4,282,266)
W. G. Gibson Signal Separation Networks (4,283,741)
E. A. Goldberg Degaussing Arrangement for Maser Surrounded by Magnetic Shielding (4,286,304)

S. A. Harper Method for Improving the Adherence of a Phosphor-Photobinder Layer to a Glass Support (4,284,694)
W. F. Heagerty and R. L. Pryor Folded-Cascode Amplifier Arrangement With Cascode Load Means (4,284,959)
K. G. Hernqvist Method for Coating a Selected Portion of the Internal Neck Surface of a CRT (4,285,990)
R. C. Heuner Starting Circuit for Low Power Oscillator Circuit (4,282,496)
R. J. Himics, M. Kaplan, and N. V. Desai Method of Exposing and Developing a Homopolymer Resist (4,286,050)
L. M. Hughes and K. L. George Stylus Cleaning Apparatus for VideoDisc Player (4,285,524)
A. C. Ipri Input Protection Device for Insulated Gate Field Effect Transistor (4,282,556)
E. A. James Fabrication of Videodisc Flyleads (4,284,712)
J. E. James Wide Range Drift Compensated FM Signal Generator (4,286,237)
N. Kucharewski and J. E. Gillberg Gated Oscillator (4,286,233)
A. J. Leidich Reference Current Supply Circuits (4,282,478)
A. J. Leidich Amplifier With Electrically Controlled Gain, With Output Suitable for Direct Coupling (4,286,226)
D. W. Luz and D. H. Willis Deflection and Power Supply Circuit With Reduced Start-Up Drive (4,282,460)
E. F. McKeon Switching Network (4,284,911)
E. B. Priestley and P. J. Call Method of Depositing a Silicon Oxide Dielectric Layer (4,282,268)
R. L. Pryor and W. F. Heagerty Folded-Cascode Amplifier Arrangement With Current Mirror Amplifier (4,284,958)
G. D. Pyles, J. A. Wilber, and T. J. Christopher Fast Recovery Squelch Circuit for a VideoDisc Player (4,286,290)
F. R. Ragland, Jr. Method for Determining the Average Width of Luminescent Stripes of a Viewing Screen (4,286,164)
G. A. Reitmeier Television Image Size Altering Apparatus (4,282,546)
R. N. Rhodes Checkerboard Color Filter Providing Tolerance (4,286,285)
E. A. Rutishauser NTSC to PAL Transcoder (4,283,738)
R. F. Sanford Automatic Shutdown Arrangement for Stand-Alone Television Modulator (4,286,336)
P. B. Simon and R. L. Barbin Television Raster Centering Aid (4,282,461)
P. D. Southgate Apparatus for Discerning the Noticeable Presence of Spatial Fluctuations of Intensity Within a Two-Dimensional Visual Field (4,282,510)
P. D. Southgate and H. N. Crooks Apparatus for Discerning the Noticeable Presence of Spatial Fluctuations of Intensity Within a Two-Dimensional Visual Field (4,282,511)
F. Sterzer Ridge-Waveguide Applicator for Treatment With Electromagnetic Energy (4,282,887)
J. Tults Keyboard Encoding Arrangement (4,282,516)
J. A. VanRaalte Modular Tube Shadow Mask Support System (4,283,654)
J. A. Wilber and T. J. Christopher VFO Having Plural Feedback Loops (4,286,235)

September

J. M. Assour, T. I. Bates, J. R. Bender, and J. M. Neilson Semiconductor Thyristor Device Having Integral Ballast Means (4,292,646)
D. S. Binge Hinge Construction With Positive Locking Means (4,290,168)
W. Bohringer Regulated Deflection Circuit With Start-Up and Electronic Circuit Breaker Control (4,291,257)
C. W. Carter Controlled Local Oscillator With Apparatus for Extending Its Frequency Range (4,288,875)
B. R. Clay Technique for Recording a Hologram Suitable for Use in Optical Retrieval System (4,289,372)
R. R. Demers Wafer and Boule Protection During the Blade Return Stroke of a Wafer Saw (4,287,256)
J. J. Hanak Laser Processing Technique for Fabricating Series-Connected and Tandem Junction Series-Connected Solar Cells Into a Solar Battery (4,292,092)
J. G. N. Henderson and R. J. Maturo Search Type Tuning System With Direct Address Channel Selection Apparatus (4,291,413)
K. G. Hernqvist CRT With Means for Suppressing Arcing Therein (4,288,719)
P. M. Heyman and D. P. Bortfeld Apparatus and Method for Reading an Identifying Label on an Information Record (4,292,511)
H. C. Johnson Interrogating Radar for Use With Tagged Targets (4,292,637)
S. W. Kessler, Jr. and J. A. Olmstead Semiconductor Power Device Having Second Breakdown Pro-

tection (4,291,324)

R. F. Kolc Nozzle for Dispensing Viscous Fluid (4,291,642)

W. J. Maddox Light Transmission Measurement Method (4,289,406)

M. J. Mindel, M. E. Miller, J. C. Rustman, and R. C. Palmer Method for Improving the Quality of Low Frequency Output of a VideoDisc Pickup Stylus (4,287,689)

S. V. Naimpally Luminance and Chrominance Signal Separation Network (4,288,811)

E. J. Nossen System and Method for Frequency Discrimination (4,291,269)

E. J. Nossen Frequency Demodulation System (4,291,275)

R. N. Rhodes Color Filter (4,288,812)

R. N. Rhodes, A. C. Schroeder, and W. H. Moles Color Encoding Filter (4,290, 671)

R. L. Rodgers, 3rd Relaxation Oscillators With Electrical Control of Periodicities of Oscillation (4,292,605)

R. L. Shanley, 2nd Composite Keying Signal Generator for a Television Receiver (4,291,336)

E. D. Simshauser and R. W. Nosker Signal Loss Detector for Video Disc (4,287,587)

B. W. Siryj and A. P. Gilson Optical Disc Changer Apparatus (4,286,790)

P. D. Southgate Inspection System for Detecting Defects in Regular Patterns (4,292,672)

S. A. Steckler and A. R. Balaban Deflection System and Switched-Mode Power Supply Using a Common Ramp Generator (4,292,654)

P. K. Weimer Architecture Line-Transfer CCD Imagers (4,291,239)

W. C. Young Assembly for Positioning the Coupling Probe of a Waveguide (4,287,496)

D. H. Ziegel Work Holder (4,286,414)

AUTHORS

Robert E. Askew was awarded a BSEE degree from the Newark College of Engineering, where he also attended graduate courses. He joined RCA's Microwave Tube Operation in 1961. After an assignment in the pencil tube design and applications group, he worked on microwave solid-state design projects as part of the Advanced Development activity, where he developed solid-state oscillators for radiosonde applications and projectile telemetry transmitters. He transferred to the RCA Solid State Division, where he supervised the fabrication and test of microwave power amplifiers for military and space applications. In addition, he served as type engineer for thick- film hybrid devices used in heart pacers. After a stay at Microwave Semiconductor Corporation in 1977/1978, Mr. Askew returned to RCA Laboratories' Microwave Technology Center, where he is currently engaged in the design of state-of-the-art microwave low-noise amplifiers and down converters and other advanced microwave components.

He has published several papers on microwave solid-state components, and has been awarded two patents. He is a Member of the IEEE and of its Professional Group on Microwave Theory and Techniques.

Philip C. Basile received a BEE from Pratt institute in 1972. He then joined RCA where he was involved in rf and analog design of receive circuits for SHF communications terminals. In 1975 he joined the Magnavox Company in the design of receiver and upconverter circuits from HF through L Band. He also worked on HF and UHF analog design with ITT. Since his return to RCA in 1980, he has been involved in rf design and integration of communications equipment from VLF through UHF for the ICS Engineering group on IR&D and the Trident program.

Daniel W. Bechtle received a BA (Honors) in Physics from the University of Oregon in 1971 and a PhD degree in Physics in 1977 from the University of Colorado. As part of his graduate work, he designed and built an automatically stabilized scanning Fabry-Perot interferometer. His PhD dissertation was concerned with experimental laser-light scattering in a transparent semiconductor. While at the University of Colorado he also consulted for Burleigh Instruments. He has designed one of two electronic instruments that received an IR-100 award from *Industrial Research* magazine in 1976. In 1978 he joined RCA Laboratories at Princeton, NJ, as a Member of Technical Staff. There he has developed analog and digital fiber-optic communication systems for studio video applications, and is currently developing a 1-GHz optical delay line.

Dr. Bechtle is a member of Phi Beta Kappa. He is the author of six papers and presentations.

Eugene P. Bertin received the PhD in Analytical Chemistry in 1952 at the University of Illinois and remained there as an Instructor in Chemistry until 1953. In 1953, he joined RCA Corporation in Harrison, NJ, where he had charge of application of x-ray radiography, diffraction, and spectrometry to the development, manufacture, and testing of receiving-type electron tubes and of semiconductor, thermoelectric, and cryogenic materials and devices. In 1969 he joined RCA Laboratories in Princeton, NJ, where he has charge of electron-probe microanalysis. Dr. Bertin is a member of the American Chemical Society, Electron Microscopy Society of America, Microbeam Analysis Society, and Society for Applied Spectroscopy. His publications include some 30 papers and articles in the field of x-ray fluorescence spectrometry and two books, "Principles and Practice of X-Ray Spectrometric Analysis" and "Introduction to X-Ray Spectrometric Analysis."

Joseph E. Brown attended the Indiana Institute of Technology during the years from 1967 to 1969 and served in the U.S. Army from 1970 to 1972. He then joined the RCA Laboratories in 1973 where he has been engaged in computer controlled measurements, mechanical design, and assembly of semiconductors for microwave circuits. He is presently a Senior Technical Associate of the Laboratories. His present interests include design of microwave components, and software and hardware development for computer-controlled rf measurement systems.

Raymond L. Camisa received his BEE, MEE, and PhD degrees from the City College of the City University of New York in 1965, 1969, and 1974, respectively. From 1965 to 1967 he was at the RCA Advanced Communications Laboratory, New York, where he worked on microwave filters, low-noise parametric amplifiers, and microwave integrated-circuit techniques. From 1967 to 1970, as a Member of Technical Staff at Wheeler Laboratories, Inc., Great Neck, LI, he was part of a group developing a microwave integrated-circuit receiver for IFF applications. Specifically, he developed various MIC components including low-noise transistor amplifiers, frequency multipliers, and filters. From 1970 to 1974 he was a part-time lecturer teaching courses in electromagnetic theory, electronics, and microwave measurements. At the university, he also worked as a graduate research assistant investigating the use of MIS varactors in microwave networks. During those years he was a consultant to Wheeler Laboratories and the RCA Advanced Communications Laboratory. In 1974 Dr. Camisa joined the Microwave Technology Center at RCA Laboratories. His responsibilities include research on GaAs field-effect-transistor device technology and linear-amplifier development.

Dr. Camisa has published numerous papers on microwave devices and systems and currently holds two U.S. patents.

Dr. Camisa is an active member of IEEE and has served on many committees on the local chapter level. He is a past chairman of the MTT/ED Princeton section and is a member of Sigma XI.

Martin Caulton received his BS, MS, and PhD degrees, all in Physics, from Rensselaer Polytechnic Institute, in 1950, 1952, and 1954, respectively. He completed his doctoral research at the Brookhaven National Laboratories in high-energy nuclear physics. From 1954 to 1955 he was a Fulbright scholar at the Imperial College of Science and Technology in London. In 1955, he joined the Technical Staff at Bell Telephone Laboratories working in research and development of low-noise microwave tubes. In 1958 he became Assistant Professor of Physics at Union College, Schenectady, New York.

Dr. Caulton joined RCA Laboratories as a Member of Technical Staff, in 1960. There he engaged in research on microwave power tubes, multivelocity flow problems in electron beams and plasmas, and microwave solid-state devices. He has been directing projects in microwave integrated circuits since 1966, and has authored numerous papers in this field. In 1968 and 1971 he was the recipient of RCA Laboratories' Achievement Awards for this work. He has worked on the basic design and measurement of microstrip circuits and integration methods based on the use of lumped elements for the miniaturization of high-power amplifiers and microwave circuits, including FET devices. He was elected a Fellow of the IEEE in recognition of his work.

Dr. Caulton has coauthored a textbook, *Physical Electronics* (John Wiley & Sons, Inc., New York, 1967), and has also taught courses in microwaves and modern physics as Adjunct Professor of Electrical Engineering at Drexel Institute of Technology. In 1971–1972 he served as Visiting Professor at the Technion (Israel Institute of Technology) in Haifa, Israel. From 1970 to 1975 he served first as Cochairman and later as Chairman of the Committee on Microwave Integrated Circuits of IEEE's Microwave Theory and Techniques Society and was formerly an Associate Editor of *Transactions of Microwave Theory and Techniques*. He is a member of the American Physical Society and Sigma Xi, and a Fellow of the IEEE.

Stuart S. Colvin, after completing four years of military duty in the U.S.A.F., joined the staff at Laser Diode Laboratory, Metuchen, NJ, where he was engaged in the work on GaAs crystal growth from 1972 to 1978. In 1978, Mr. Colvin joined the Microwave Technology Center at RCA Laboratories in Princeton, NJ, as a research technician. He has participated in the development of plasma-grown GaAs oxides and their use in MOSFET device fabrication. Most recently, Mr. Colvin has been involved in exploring the potential of GaAs and GaInAs MISFETs for microwave power and multigigabitrate logic circuits.

John F. Corboy is an Associate Member of Technical Staff at RCA's David Sarnoff Research Center, Princeton, NJ, and is a member of the Materials Synthesis Group within the Materials and Processing Research Laboratory. He joined RCA in 1959 and was engaged in the epitaxial growth of III–V compounds and also in the synthesis and crystal growth of organic compounds. From 1965 to 1980, he studied the properties of silicon on insulating substrates and was involved in the transfer of silicon-on-sapphire technology between RCA Laboratories and other divisions of RCA. Currently, he is involved in silicon homoepitaxy and in plasma etching of oxide films.

Mr. Corboy has been issued two U.S. patents and was the recipient of an RCA Laboratories Achievement Award in 1974.

Richard G. Erdmann received a BSEE from Purdue University and joined RCA in 1950. He has worked with airborne HF and UHF command sets for USAF tactical use. He also worked on X-band receiver development and UHF data and communications equipment for the Gemini and Apollo manned space programs. He has been involved with recent developments in secure communications equipment design and UHF satellite terminal design for the Air Force. Most recently, he has been working in the field of Integrated Computer Controlled Radio Systems for the Navy's Trident program in the areas of antenna switching and HF/UHF communications. He is a member of Eta Kappa Nu, Tau Beta Pi and the IEEE.

Peter D. Gardner received the BSc degree in Applied Physics from Brunnel College of Advanced Technology, London, England, in 1960. From 1960 to 1961, at Transitron Electronic Corp., he was engaged in developing very low temperature coefficient zener diodes and very low voltage zener diodes. Mr. Gardner joined the RCA Solid State Division at Somerville, NJ, in 1961 and has worked in various areas of semiconductor devices, including very high speed tunnel diodes for switching and very high power tunnel diodes for power conversion. He was responsible for the group that developed processes for fabricating integrated complementary-symmetry MOS devices. Later he was responsible for an advanced technology group developing basic processes for LSI fabrication and improved semiconductor devices, including silicon preparation techniques, diffusion, ion implantation, CVD, clean oxidation, photoresist, and metallization. Mr. Gardner transferred to the Linear IC Product Group in 1970 and was responsible for the development of new technology and processes for linear integrated circuits and very high speed ECL digital circuits. He later held posts in government marketing. Mr. Gardner joined the RCA Microwave Technology Center at Princeton, New Jersey, in 1978 and is working on high-speed GaAs digital integrated-circuit technology.

He has authored several papers in the field of tunnel diodes and MOS integrated circuits, and was corecipient of the 1977 David Sarnoff Team Award in Science for the development of CMOS LSI circuits.

Yehoshua Gazit graduated from the Technion, Israel Institute of Technology, with a BS degree in 1973. He then joined Rafael, Haifa, Israel. As a project engineer he was involved with the development of power amplifiers, VCO's, up-converters, and numerous other solid-state radar components. During the period April 1980–June 1981, he was on leave working at RCA Laboratories on cascadable X-band power amplifiers for satellite applications and on the Ku-band phase shifter. He is now head of the Microwave Sources group at Rafael.

Anna M. Gombar was born in Hungary. After attending the Technical University in Budapest, she came to the United States in 1956. In 1960 she began textile research at FMC in Princeton, NJ. Transferring to RCA Laboratories in 1973, she was engaged in research in the field of silicon devices such as high-power p-i-n diodes, high *Q* varacter diodes, and lately, millimeter wave device technology. She is the holder of several U.S patents and the author of several technical publications.

Demetrios Haggis received his BS degree in Physics from Athens University, Athens, Greece; his MS degree in Physics from Northeastern University, Boston, Mass.; and his PhD in experimental solid state Physics from Northeastern University, Boston, Mass. He studied electron mean free paths at low temperatures of very pure metals. He joined RCA, Burlington, in 1979, working in the hybrid facility as a process engineer with interests in computers and failure analysis.

He is a member of ISHM.

Walter Janton served in the U.S. Army as a Communications Technician from 1939 to 1945. In 1948 he graduated from the Baronian School of Horology, Philadelphia, PA. From 1953 to 1959 he was a Senior Research Technician at Bell Telephone Laboratories, Murray Hill, NJ, in the Model Tube Laboratory. In 1959 he transferred to SFD Research Laboratory (Varian Associates). He joined RCA Laboratories in Princeton, NJ in 1972 as a Research Technician. He has worked on the electron tube injected beam transistor program and cathode-luminescent display devices. For the past three years, he has been responsible for the mechanical design and fabrication of work on the millimeter-wave, p-i-n, and varactor diode projects.

Henry Johnson attended Johns Hopkins University and received the BS Degree from Drexel University. He joined the RCA Electron Tube Division in Harrison, NJ in 1956 working on pencil tube design. In 1959, he transferred to the Microwave Technology Center at the RCA Laboratories in Princeton, NJ, where he has made significant contributions in the fields of optical communications and microwave transistor and bulk device circuitry. He has successfully completed programs involved with the development of microwave sources, FET phase shifters, and radar transponder systems. More recent responsibilities include the design of a microwave synthesizer, an active antenna array, and the development of pulse-compression and FM-CW radars. He was the recipient of RCA Laboratories Achievement Awards in both 1978 and 1979.

Mr. Johnson holds 10 patents and has contributed more than 30 papers to technical journals of conferences.

S. T. Jolly received his BSc degree in Metallurgy from the University of Wales in 1939. From 1946 to 1952 he was employed by EMI Ltd., supervising the materials and components test and evaluation laboratory. Since 1953 he has been employed by RCA, initially as Engineering Leader responsible for the development of computer hardware. As Manager of the Magnetic Head Design Department from 1959 to 1963, he supervised the design and development of all magnetic recording heads for professional audio, video, and digital recording. From 1963 to 1968, Mr. Jolly was an Engineering Group Leader with RCA Defense Electronics Products, responsible for developmental work in computer memories, automated test equipment, for computer tape recorders, and production of high-resolution photomasks for IC devices. Mr. Jolly was the Senior Engineer responsible for the initial design and process development of liquid-crystal displays.

He is currently working on the development of epitaxial-growth processes and the pro-

duction of gallium arsenide for solid-state microwave devices with the Microwave Technology Center located at the David Sarnoff Research Center in Princeton, New Jersey. In this assignment he has developed processes for the growth of thin (less than 1-mm thickness) multiple layers required in the fabrication of growing chromium- and oxygen-doped buffer layers on semi-insulating GaAs substrate material.

Mr. Jolly holds two patents in the field of magnetic memories and magnetic recording, and one patent concerned with the construction of vapor-phase reactors.

Jerome B. Klatskin received his BS degree from Trenton State College in 1972 and has done graduate work at Rider College, Trenton, NJ. From 1959 to 1962, when he was employed by Princeton University, he was engaged in the development of electronic equipment for Plasma-Physics Research. In 1962 Mr. Klatskin joined RCA's Microwave Technology Center to work on TWT development. In military service from 1965 to 1969, he served as a pilot and Instrument Flight Instructor. Rejoining RCA in 1969, he worked on IMPATT, TRAPATT, and device fabrication.

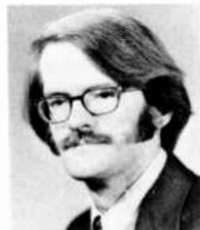
A Member of Technical Staff, Mr. Klatskin is presently working on FET circuit development for X-band and Ku-band frequencies. He has been awarded three patents and has two patent pending. Mr. Klatskin is a member of IEEE.

Mahesh Kumar received his MS in Physics from the Agra University, Indian, in 1971; his MS in Electronics from Birla Institute of Technology and Science, Pilani, India, in 1973; and his PhD in Electronics from Indian Institute of Technology, Kharagpur, India, in 1977. From 1976 to 1978, he was a faculty member at Radar and Communication Center, Indian Institute of Technology, where he was involved in the development of stripline components for Phase Array Radar. In October 1978, he joined the Microwave Technology Center at RCA Laboratories, Princeton, NJ, as a member of Technical Staff, where he is engaged in research and development of GaAs Monolithic Microwave Integrated Circuits. He has published several papers on stripline/microstrip components, dual-stage FET amplifiers, phase shifters, etc.

Dr. Kumar is a member of IEEE and past Chairman of MTT/ED Chapter of the Princeton section.

Shing-gong Liu received the BS degree in Electrical Engineering from Taiwan University, Taipei, Taiwan, in 1954, the MS degree in Electrical Engineering from North Carolina State College, Raleigh, in 1958, and the PhD degree in Electrical Engineering from Stanford University, Stanford, California, in 1963. From 1958 to 1959, he worked with IBM Laboratories, Poughkeepsie, New York; from 1960 to 1963, he did research work on microwave ferrites in the Hansen Microwave Laboratories, Stanford University. At RCA Laboratories, Princeton, New Jersey, which Dr. Liu joined in August 1963, he has been engaged in research on the use of high-field nonlinear effects in GaAs for microwave devices and optical modulation, beam deflection devices, and avalanche-diode microwave oscillators, using both Si and GaAs materials. From 1974 to 1976, he has worked on high-efficiency solar cells for concentrator application and on GaAs Schottky diodes for low-noise mixers for satellite ground stations. Since 1977 he has been working on ion implantation in GaAs material and on the development of field-effect transistors containing ion-implanted material. He received three RCA Outstanding Achievement Awards for his work on high-power high-efficiency avalanche diodes.

Dr. Liu is a member of Phi Kappa Phi, IEEE, Sigma Xi, and the American Physical Society.



Charles W. Magee was graduated by the University of Virginia with a BS degree in Chemistry in 1969, and with a Ph.D in 1973. While in graduate school he concentrated on electrical methods of ion detection in spark-source mass spectrometry. He joined the Technical Staff of RCA Laboratories immediately upon completion of his graduate work and is presently a member of the Materials Characterization Research Group. His work deals mainly with the trace-elemental analysis of thin solid films by means of secondary-ion mass spectrometry for which he received an Outstanding Achievement Award in 1976. In 1979 he received the Young Author Award of the Electrochemical Society. Dr. Magee has authored over 50 publications on SIMS and is an active member of the American Society for Mass spectrometry. He is currently chairman of the Solids and Surface Analysis Committee of the ASMS. In addition, Dr. Magee is a member of the American Vacuum Society and serves on the steering committee for the Greater New York Chapter having been its chairman in 1980. He is also a member of Sigma Xi.

Richard E. Marx attended Rutgers University, Fairleigh Dickinson University and West Coast University for a BSEE. He joined RCA Microwave Tube Operation, Harrison, NJ, in 1959 where he worked on magnetrons, TWTs and tunnel-diode oscillators. In 1960 he was transferred to RCA's Microwave Engineering Operation in Los Angeles, CA, where he participated in the development of solid-state frequency multipliers used in the LEM project. Mr. Marx returned to RCA Harrison in 1964 to participate in the production of the LEM radar units. In 1966 he joined the Microwave Technology Center at RCA Laboratories, Princeton, NJ, as an Associate Member of the Technical Staff where he has worked on device technology, TEOs, computer aided design systems, solar energy, and small radar and radar systems. Mr. Marx holds two patents.

Ralph J. Matarese attended Trenton Junior College and Mercer County Community College (Evening Division) in New Jersey. Mr. Matarese joined RCA Laboratories, Princeton, New Jersey, in 1962. Currently, he is a Senior Technical Associate in the Microwave Technology Center. He has been engaged in circuit construction, photolithographic processing of silicon and mercury-cadmium-telluride infrared-imaging devices, gallium arsenide research on Schottky-barrier FETs. "Traveling Wave" transistors and currently, GaAs MSI technology.

Mr. Matarese has been granted one patent and another is pending.

A. Mikelsons has been with RCA since 1956. His career with RCA started at the Surface Communications Systems, Lab in NY which later became the Advanced Communications Laboratory. While there he participated in the development of microwave components for a broad spectrum of applications, including ground to missile, and satellite to ground communications systems. He was a contributor to the development of upconverters and downconverters for army small satellite terminals. He also was a contributor in many broadband parametric amplifier programs.

In 1976 Mr. Mikelsons joined RCA Laboratories in Princeton as a Research Technician, where he has worked on the circuit aspects of microwave GaAs FET power amplifiers. He has participated in the development of both narrow band and braodband FET amplifiers. He currently is involved in the development of lumped-element matching and distributed combining techniques as applied to broadband FET amplifiers.

S. Yegna Narayan received his BSc (Honors) from the University of Delhi, India, in 1959; his BE with Distinction from the Indian Institute of Science, Bangalore, India, in 1962; and his MS and PhD degrees from Cornell University in 1964 and 1966, respectively. His graduate research dealt with the coupling of microwave energy to electron beam-plasma systems. Since joining RCA in 1966, Dr. Narayan has been working mainly in the area of semiconductor microwave devices such as GaAs transferred-electron devices, Schottky-barrier devices, high-quality GaAs varactor diodes, GaAs field-effect transistors, and multigigabit-rate logic technology. Dr. Narayan, as Head, Microwave Device Technology, has responsibility for the development of compound semiconductor microwave devices at the Microwave Technology Center, RCA Laboratories, Princeton, NJ.

Dr. Narayan was the recipient of two RCA Laboratories Outstanding Achievement Awards; one in 1968 for his work in the development of GaAs transferred-electron device technology and the other in 1972 for the development of high-quality GaAs varactor diodes. He has also been issued five U.S. patents. Dr. Narayan is a Senior Member of the IEEE and a member of the American Physical Society.

John Paczkowski graduated from the Polytechnic Institute of Brooklyn, NY, with a BS in Physics in 1968. He is currently working on GaAs materials technology at the Microwave Technology Center of RCA Laboratories, Princeton, NJ. He was a key contributor to the development of the integral heat sink technology for transferred electron devices and the development of GaAs varactors. He was awarded an RCA Laboratories Achievement Award in 1972 for his contribution to the development of GaAs varactors for television tuner applications. Before his current assignment, he was responsible for the operation of a 3-bay processing area at the Microwave Technology Center.

John Paczkowski has 2 patents and is co-author to several technical publications on GaAs device technology.

Barry S. Perlman received the BEE from the City College of New York in 1961, and the MSEE and the PhD in Electrophysics from Brooklyn Polytechnic Institute in 1964 and 1973, respectively. He is presently Manager of CAD and Testing in the Microwave Technology Center at the RCA David Sarnoff Research Center, Princeton, NJ. His group is responsible for the development of computer aided design, advanced automated measurement techniques and other computer aids to engineering. He has published more than 30 technical papers in the fields of solid state devices, microwave networks and CAD and has received four patents. In 1969, he received an engineering achievement award for advanced device development, and in 1970 he shared an RCA Laboratories' Outstanding Achievement Award for his part of a team effort in the development of wideband transferred electron amplifiers. In 1975, he received an Achievement Award for his contribution to computer aided design and laboratory automation.

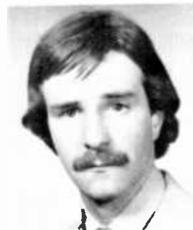
Dr. Perlman is a member of Sigma Xi, the IEEE, and a registered professional engineer in the State of New York. He is a member of the IEEE sub-groups on Microwave Theory and Techniques, Instrumentation and Measurements and on Systems and Cybernetics. He is currently President of the HP International Users Group.

Adolph Presser received the BEE degree from the Institute of Technology, Vienna, Austria, in 1950, and the MEE degree from the Polytechnic Institute of Brooklyn, New York, in 1961. In 1959, Mr. Presser joined the RCA Microwave Technology Center at RCA Laboratories, Princeton, NJ, as a member of the technical staff. As a member of the Microwave Electronics section of this group, he has been engaged in the development of various solid state microwave devices. His work includes the design and development of parametric amplifiers, tunnel diode amplifiers, tunnel diode frequency converters, and tunel diode oscillators. In 1965, Mr. Presser's field of interest shifted towards microwave integrated circuitry. He was instrumental in the design and development of telemetry transmitters, high-power transistor amplifiers, power sources for ECM systems, linear transistor power amplifiers and Doppler radar modules. More recently he developed varactor tunable resonant elements for test tuning active microwave filters.

Mr. Presser received an RCA Laboratories Outstanding Achievement Award in 1965 and 1976. He is the author and co-author of many papers in the field of solid state components and is the holder of several US patents.

Michael Rauchwerk received the BSEE degree in 1978 and MSEE degree in 1980, both from Rutgers University.

Since joining Missile and Surface Radar in 1979, Mr. Rauchwerk has been involved in various projects concerned with Radar Signal Processing, FFT Spectrum Analysis, Digital Filtering, Real-Time data acquisition and analysis and associated microprocessor implementations. From 1978 to 1979 he was a Research Assistant at Rutgers University involved with Digital Image Processing.



David L. Rhodes received his BSEE degree from Rutgers University, College of Engineering in 1980 and is presently working toward a MSEE degree at Princeton University under the RCA Graduate Study Program. He joined the Microwave Technology Center at RCA Laboratories in 1980 and has been working in the field of microwave modelling and simulation as well as microwave CAD. Recently, he has been concurrently active in computer graphics and developing highly accurate models for power dividers.

Mr. Rhodes is a member of Eta Kappa Nu, Tau beta Pi and IEEE.

Arye Rosen received the BSEE degree cum laude from Howard University in 1963 and the MScE degree from Johns Hopkins University (which he attended on a Gillman Fellowship) in 1965. He was an instructor at Johns Hopkins during 1963–64. From 1964 to 1967, Mr. Rosen was concerned with systems design at General Telephone and Electronics International, and with antenna and circuit design at Channel Master, Inc., and American Electronics Laboratories, Inc. In 1967, Mr. Rosen joined RCA Laboratories, where he is presently engaged in the study and development of microwave circuits and devices. He is the recipient of a 1972 RCA Laboratories Outstanding Achievement Award for a team effort in the development of S-band TRAPATT amplifiers. From 1970 to 1971, on leave of absence from RCA, Mr. Rosen was engaged in research in the Division of Cardiology at Jefferson Medical College in Philadelphia, Pennsylvania, where he received the degree of MSc in Physiology and where he presently holds an appointment as an Associate in Medicine. Mr. Rosen is the author of over 30 technical papers and presentations and holds 18 patients in the microwave field; he is also the author of several papers and presentation in the field of echocardiography.

He is a member of Tau Beta Pi, Sigma Xi, and the Association of Professional Engineers of British Columbia.

Jerome Rosen received his BSEE degree in 1969 and his MSEE degree in 1972, both from Newark College of Engineering. Since 1957 he has been engaged in research and development of microwave devices and subsystems in the frequency range of 30 MHz to 40 GHz, including filters, couplers, discriminators, ferrite phase shifters, diode phase shifters, YIG filters, "lumped element" equivalents of microwave hybrids for VHF, and an instantaneous frequency measurement (IFM) receiver. Mr. Rosen is currently a member of the Microwave Technology Center at RCA Laboratories. Since 1969, when he joined the Laboratories, his assignments have included the development of strip-line antenna arrays and reflectors; an integrated dual-frequency antenna and low-power doubler for the electronic tag of a microwave automatic vehicle identification (AVI) system; a microstrip transmitter for an electronic signpost (AVM) system; and the microwave front end of an automotive radar for collision avoidance and headway following.

Mr. Rosen is a member of IEEE and PGMTT. He has authored several technical papers and holds a patent on an improved design of a millimeter wave oscillator.

Franco N. Sechi received the degree of Doctor in Electrical Engineering in 1964 from the Polytechnic Institute of Milano, Italy. From 1965 to 1968 he was employed by ITT in Milano, where he was concerned with the design of solid-state microwave radio-link equipment. In 1968, he joined RCA, Electronic Components, as a design engineer in the Solid State Product Design Group. In this position he designed transferred-electron oscillators and developed a technique for measuring the impedance of transferred-electron diodes under large-signal conditions. In 1973, he transferred to the Microwave Technology Center, RCA Laboratories, Princeton, NJ. In his present position he is involved in the development of power transistor amplifiers. For his work on linear microwave power amplifiers, he received an RCA Laboratories Outstanding Achievement Award in 1976. He received a second Achievement Award in 1979 for his work on a solid-state radar system for aircraft.

Dr. Sechi has authored papers on transferred-electron oscillators, the thermal and large-signal characterization of microwave devices, and high-power microwave transistor amplifiers. He currently holds six U.S. patents. Dr. Sechi is a member of the IEEE.

Rene Smith was born in Surabaja, Indonesia. He went to the Netherlands where he attended the Technical School in Amsterdam. He served in the Royal Dutch Army for two years. He was with Transitron Electronic Corporation in Massachusetts from 1959 to 1965 and with Itek Corporation from 1965 to 1966. He has been with the RCA Laboratories since 1966, and is involved in research and development of various silicon semiconductor devices, GaAs varactor diodes, Gunn diodes and GaAs integrated circuits.

Ronald T. Smith joined RCA Laboratories as a Research Technician in 1963 after receiving a BS in Physics from Moravian College of Bethlehem, Pa. He has studied as a part-time graduate student in the Department of Materials Science of the University of Pennsylvania completing three courses and the basis for a Masters Thesis. The Masters Thesis work has involved the solving of the crystal structure of YWO_2Cl. He is presently a member of the Materials Characterization Group specializing in single-crystal x-ray diffraction studies. This area includes Laue, Weissenberg, pole-figure, and diffractometry techniques as well as computer-related data reduction programming. He has recently concentrated on the means for the characterization and qualitative comparison of thin films.

Since working at the Laboratories, he has published eight papers.

Paul Stabile received the B.E. degree in electrical engineering summa cum laude from Manhattan College in 1979. Afterward, he entered the Engineering Rotation Program at RCA. His assignments included microwave amplifier design, digital circuit development, and a study of VLSI computer aided design techniques. In October 1979, he joined RCA Laboratories, where he is presently an Associate Member of Technical Staff. There he has been engaged in research of high power, low-frequency p-i-n diodes, and silicon millimeter wave devices, and integrated circuits. He is also the author of several technical papers.

Mr. Stabile is a member of Eta Kappa Nu, Tau Beta Pi, and Epsilon Sigma Pi of Manhattan College.

Fred Sterzer received the BS in Physics from the City College of New York in 1951, and the MS and PhD degrees in Physics from New York University in 1952 and 1955, respectively. His PhD thesis was on microwave spectroscopy. He joined RCA in 1954 and has worked there on the development of traveling-wave tubes, optical components, high-speed logic, and microwave solid-state devices and circuits. His most recent work involves the application of microwave heating to the treatment of human cancers.

Dr. Sterzer is currently Director of the Microwave Technology Center at RCA Laboratories, leading a group of approximately 85 scientists, engineers and technicians engaged in developing new microwave technologies. He is a member of the N.J. Commission on Radiation Protection and Chairman of its Advisory Committee on Non-ionizing Radiation.

Dr. Sterzer is a Fellow of the IEEE and a member of Phi Beta Kappa, Sigma Xi, and the American Physical Society. He is the author of over 75 papers and holds more than 30 patents.

Gordon Taylor received the BS, MS, and PhD degrees in Electrical Engineering in 1969, 1972, and 1976 from Rutgers University. His PhD thesis was on switching and conduction mechanisms of polycrystalline thin films of TiO_2. From 1976 to 1977 he was employed by the Electronic Technology Division of the National Bureau of Standards in Washington, DC. During this time he engaged in the design of test structures and test patterns for integrated-circuit process monitoring and analysis. Dr. Taylor joined RCA in 1977. Since then he has worked on the development of device fabrication technology for GaAs field-effect transistors.

He has authored and coauthored several papers on the conduction, switching, and rf oscillations in TiO_2 thin films and on the optical and structural properties of co-sputtered thin films. He is a member of Tau Beta Pi, Eta Kappa Nu, IEEE, and the American Vacuum Society.

L. C. Upadhyayula received the BSc degree in Physics and the MSc in Applied Physics from Andhra University, India, in 1955 and 1958, respectively, and the PhD in Engineering from Brown University in 1968. During 1958–59, he was a trainee in the Atomic Energy Establishment, Bombay, India. From 1959 to 1964, he worked in the Electronics Division of the Atomic Energy Establishment. His work was in the area of nuclear electronic instrumentation. From 1964 to 1967, he was a research assistant and teaching assistant in engineering at Brown University, where he was engaged in the study of electrical transport properties of semiconductors. During 1968–69, Dr. Upadhyayula was a Post Doctoral Fellow in Engineering at Brown University, studying tunneling through superconducting metal-insulator-metal structures at cryogenic temperatures.

In 1969, Dr. Upadhyayula joined the Microwave Technology Center at RCA Laboratories in Princeton, New Jersey, as a Member of Technical Staff. His work at RCA includes transferred-electron amplifiers (TEAs) and oscillators, high-efficiency IMPATTs, transferred-electron logic devices, gallium arsenide field-effect transistors, and high-speed logic circuits. He is currently engaged in the development of GaAs MESFET technology for MSI and LSI logic circuits working at clock rates above 1–2 GHz. He has published several technical papers in these areas.

In 1970, he received an RCA Laboratories' Outstanding Achievement Award for a team effort in the development of GaAs transferred-electron amplifiers. He is a member of Sigma Xi and IEEE. He has been issued ten U.S. patents.

Herbert J. Wolkstein received his BSEE in 1953, and has completed his work toward an MSEE at Newark College of Engineering. From 1948 to 1955, as Project Engineer in the Research Laboratories of National Union Electric Corporation, he worked on the design of special-purpose beam-deflection and high-speed computer-switching tubes. At RCA's Microwave Tube Operations Department, which he joined in 1955, Mr. Wolkstein designed and developed traveling-wave tubes (TWTs). In 1958, he became Engineering Leader in charge of the development of TWTs and, in 1961, was promoted to the position of Manager, TWT Design and Development. In 1964, as Manager of Microwave Advanced Product Development, Mr. Wolkstein directed a group in advanced development and applications work on TWTs and solid-state devices. In 1972, he was named Manager of the Advanced Programs and Application Engineering

Group. He held that position until 1975, when he joined the Microwave Technology Center, RCA Laboratories, Princeton, NJ. In his present position of Manager, Space and Countermeasure Programs, Mr. Wolkstein is engaged in the development and applications of solid-state microwave devices and subsystems.

Mr. Wolkstein has been awarded ten patents in the electron-tube and solid-state fields. He has written numerous papers on microwave TWT and solid-state system designs. He is a member of IEEE's Professional Group on Electron Devices and Professional Group on Microwave Theory and Techniques.

Chung P. Wu received the BS, MS, MPhil, and PhD degrees in Physics from Yale University in 1965, 1966, 1967, and 1968, respectively. He was a research staff physicist at the Yale Electron Linear Accelerator Laboratory from 1968 to 1970, working on photonuclear reactions and neutron time-of-flight spectroscopy. From 1970 to 1972 he was an Assistant Professor of Physics at Nanyang University in Singapore. Since 1973, Dr. Wu has been a Member of Technical Staff at RCA Laboratories, Princeton, NJ. He has worked on different techniques for determining the electrically active ion-implanted doping profiles, the utilization of ion implantation in the fabrication of semiconductor devices, and the characterization and evaluation of such devices. He is currently working on the laser annealing of semiconductor materials, including polysilicon, crystalline silicon, SOS, and GaAs, for the fabrication of solar cells, devices, and circuits.

Dr. Wu has more than 20 technical publications and 15 patents granted or pending. He is a member of the American Physical Society, IEEE, and Sigma Xi.

Yong-Hoon Yun received the BS degree in Engineering from the Seoul National University, Seoul, Korea in 1971. He received the MS and PhD degrees in Physics from Brown University, Providence, RI, in 1974 and 1977, respectively. During 1977–1978, he was a research associate at Brown University. Since joining RCA/David Sarnoff Research Center in Princeton, NJ, in 1978, he has been working on the characterization of materials and devices for the power GaAs FETs and on developing a theoretical model of GaAs device behavior by using computer simulations. He is also engaged in research on fabrication processes of power GaAs FETs.

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